MT6328 PMIC Datasheet

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Document Revision History

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1 Overview

1.1 Features

- Handles all 2G/3G/4G smart phone baseband power management
- Input range: 2.5 ~ 4.5V
- 5 buck converters and 28 LDOs optimized for specific 2G/3G/4G smart phone subsystems
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC.
- 32K RTC oscillator for system timing, 1.8 and 2.8V clock buffer output
- Flexibility for various configurations of indicator LED current source: 2 ISINK
- SPI interface
- Li-ion battery charging function
- USB Battery Charging Specification ver 1.1/1.2 (BC1.x) Compliance
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Watchdog reset
- Flexibility hardware PMIC reset function
- Power-on reset and start-up timer
- Precision voltage, temperature, and current measurement fuel gauge
- 205-pin VFBGA package

1.2 Applications

MT6328 is ideal for power management of 2G, 3G and 4G smart phones and other portable systems.

1.3 General Descriptions

MT6328 is a power management system chip optimized for 2G/3G/4G handsets and smart phones, containing 5 buck converters and 28 LDOs optimized for specific 2G/3G/4G smart phone subsystems.

LED drivers support up to 2 channels of LEDs with independent control. Flexible control includes register mode, PWM mode and breath mode.

Sophisticated controls are available for power-up, battery charging and the RTC alarm. MT6328 is optimized for maximum battery life, allowing the RTC circuit to stay alive without a battery for several hours.

MT6328 adopts SPI interface and 2 SRCLKEN control pins to control buck converters, LDOs, and various drivers; it provides enhanced safety control and protocol for handshaking with BB.

MT6328 is available in a 205-pin VFBGA package. The operating temperature ranges from -25 to +65°C.

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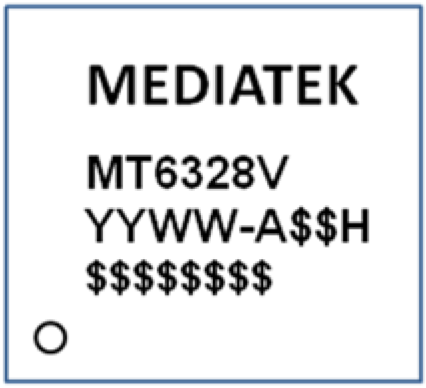
1.4 Ordering Information

Order #	Marking	Temp. range	Package
MT6328V/A		-25 ~ +65°C	VFBGA 205L

1.5 Top Marking Definition

MT6328V/A



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1.6 Pin Assignments and Descriptions

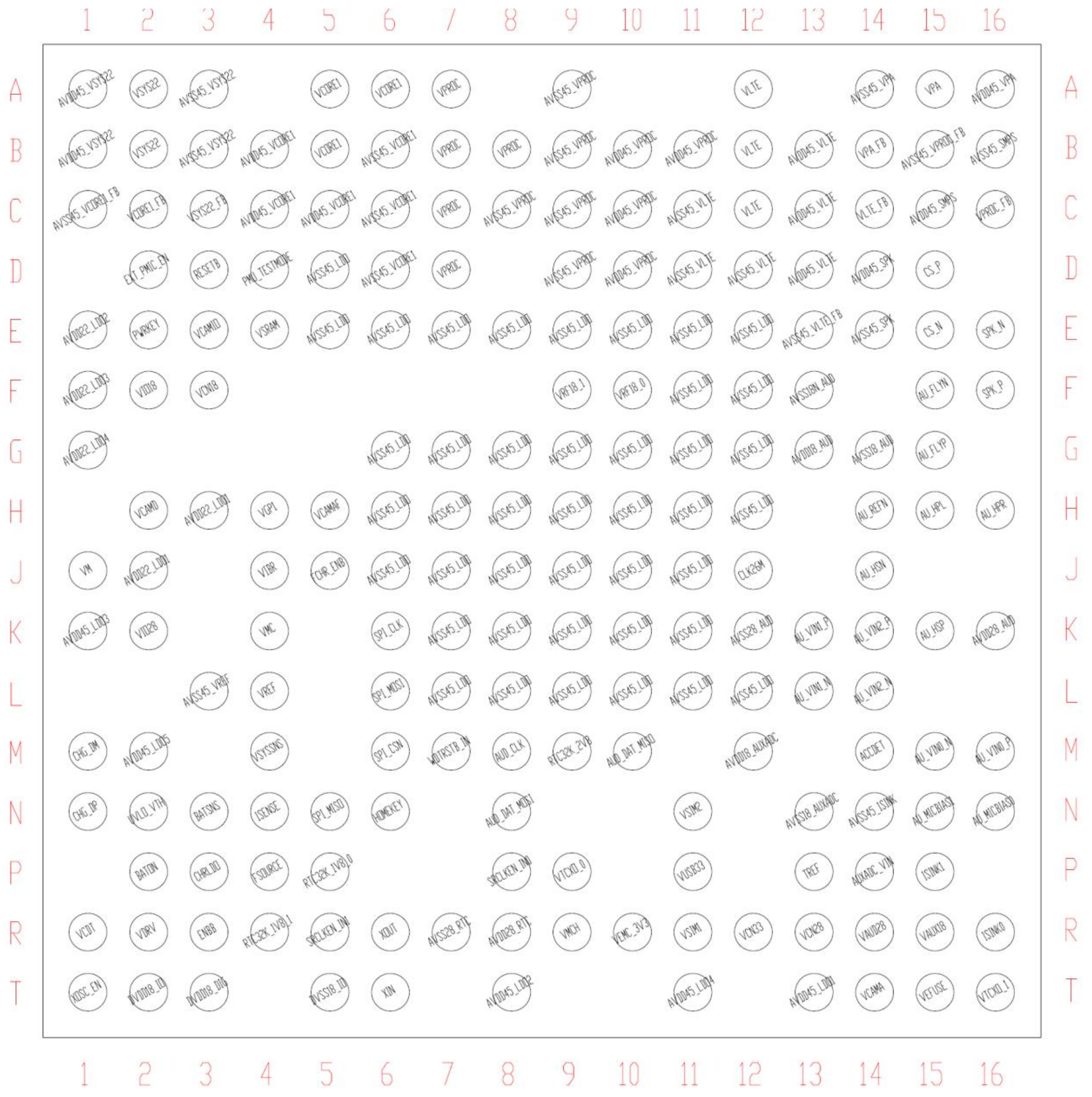

Figure 1-1. MT6328 VFBGA 205 (6.6x6.6mm) pin assignment

Table 1-1. MT6328 pin descriptions

Ball	Symbol	I/O	Description
A1,B1	AVDD45_VSYS22	PWR	Power supply of VSYS22
A2,B2	VSYS22	O	SW node of VSYS22
A3,B3	AVSS45_VSYS22	GND	VSYS22 ground
C3	VSYS22_FB	I	BUCK VSYS22 feedback pin
B4,C5,C4	AVDD45_VCORE1	PWR	Power supply of VCORE1

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Ball	Symbol	I/O	Description
A5,A6,B5	VCORE1	O	SW node of VCORE1
B6,C6,D6	AVSS45_VCORE1	GND	VCORE1 ground
C1	AVSS45_VCORE1_FB	I	Remote sense on ground of VCORE1
C2	VCORE1_FB	I	BUCK VCORE1 feedback pin
B10,B11,C10,D10	AVDD45_VPROC	PWR	Power supply of VPROC
A7,B7,B8,C7,D7	VPROC	O	SW node of VPROC
A9,B9,C8,C9,D9	AVSS45_VPROC	GND	VPROC ground
B15	AVSS45_VPROC_FB	I	Remote sense on ground of VPROC
C16	VPROC_FB	I	BUCK VPROC feedback pin
B13,C13,D13	AVDD45_VLTE	PWR	Power supply of VLTE
A12,B12,C12	VLTE	O	SW node of VLTE
C11,D11,D12	AVSS45_VLTE	GND	VLTE ground
E13	AVSS45_VLTE_FB	I	Remote sense on ground of VLTE
C14	VLTE_FB	I	BUCK VLTE feedback pin
A16	AVDD45_VPA	PWR	Power supply of VPA
A15	VPA	O	SW node of VPA
A14	AVSS45_VPA	GND	VPA ground
B14	VPA_FB	I	BUCK VPA feedback pin
C15	AVDD45_SMPS	PWR	Power supply of buck controller
B16	AVSS45_SMPS	GND	Ground of buck controller
D5,E5,E6,E7,E8,E9, E10,E11,E12,F11,F12, G6,G7,G8,G9,G10,G 11,G12,H6,H7,H8,H 9,H10,H11,H12,J6,J 7,J8,J9,J10,J11,K7,K 8,K9,K10,K11,L7,L8, L9,L10,L11,L12	AVSS45_LDO	GND	LDO ground
T13	AVDD45_LDO1	PWR	Power supply input of LDO group1
T8	AVDD45_LDO2	PWR	Power supply input of LDO group2
K1	AVDD45_LDO3	PWR	Power supply input of LDO group3
T11	AVDD45_LDO4	PWR	Power supply input of LDO group4
M2	AVDD45_LDO5	PWR	Power supply input of LDO group5
H3	AVDD22_LDO1	PWR	Power supply input of SYS LDO group1
J2	AVDD22_LDO1	PWR	Power supply input of SYS LDO group1
E1	AVDD22_LDO2	PWR	Power supply input of SYS LDO group2
F1	AVDD22_LDO3	PWR	Power supply input of SYS LDO group3
G1	AVDD22_LDO4	PWR	Power supply input of SYS LDO group4
P9	VTCXO_0	O	VTCXO_0 output voltage
T16	VTCXO_1	O	VTCXO_1 output voltage
F10	VRF18_0	O	VRF18_0 output voltage
F9	VRF18_1	O	VRF18_1 output voltage
J1	VM	O	VDRAM output voltage
E4	VSRAM	O	VSRAM output voltage
H2	VCAMD	O	VCAMD output voltage
T14	VCAMA	O	VCAMA output voltage
E3	VCAMIO	O	VCAMIO output voltage

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Ball	Symbol	I/O	Description
H5	VCAMAF	O	VCAMAF output voltage
F2	VIO18	O	VIO18 output voltage
K2	VIO28	O	VIO28 output voltage
K4	VMC	O	VMC output voltage
R9	VMCH	O	VMCH output voltage
R10	VEMC_3V3	O	VEMC_3V3 output voltage
T15	VEFUSE	O	VEFUSE output voltage
P11	VUSB33	O	VUSB33 output voltage
R11	VSIM1	O	VSIM1 output voltage
N11	VSIM2	O	VSIM2 output voltage
F3	VCN18	O	VCN18 output voltage
R13	VCN28	O	VCN28 output voltage
R12	VCN33	O	VCN33 output voltage
R14	VAUD28	O	VAUD28 output voltage
R15	VAUX18	O	VAUX18 output voltage
H4	VGP1	O	VGP1 output voltage
J4	VIBR	O	VIBR output voltage
E2	PWRKEY	I	PWRKEY button
D2	EXT_PMIC_EN	O	Ext PMIC enable pin
D3	RESETB	O	System reset release signal
M7	WDTRSTB_IN	I	Watchdog reset from AP
D4	PMU_TESTMODE	I	PMU test mode signal (tied to GND in normal operation)
L4	VREF	O	Band gap reference voltage
L3	AVSS45_VREF	GND	Ground for band gap
N5	SPI_MISO	IO	SPI control interface
L6	SPI_MOSI	IO	SPI control interface
K6	SPI_CLK	I	SPI control interface
M6	SPI_CSN	IO	SPI control interface
N2	UVLO_VTH	I	UVLO threshold control pin
N6	HOMEKEY	I	HOMEKEY button
P4	FSOURCE	PWR	EFUSE power source
P8	SRCLKEN_IN0	I	Source clock enable pin 0
R5	SRCLKEN_IN1	I	Source clock enable pin 1
M12	AVDD18_AUXADC	PWR	1.8V power supply of AUXADC
M14	ACCDET	I	Accessory detection input
P14	AUXADC_VIN	I	AUXADC input
N13	AVSS18_AUXADC	GND	AUXADC ground
N3	BATSNS	I	Negative terminal for battery's charging current sensing resistor
N4	ISENSE	I	Positive terminal for battery's charging current sensing resistor
M4	VSYSSNS	PWR	VSYS supply input for internal block and UVLO detection
N1	CHG_DP	I	USB D+ for BC1.x standard
M1	CHG_DM	I	USB D- for BC1.x standard
D15	CS_P	I	Fuel gauge ADC input pin

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Ball	Symbol	I/O	Description
E15	CS_N	I	Fuel gauge ADC input pin
J5	FCHR_ENB	I	Force charging disable pin
P13	TREF	O	TREF output voltage
R1	VCDT	I	Fractional charger input voltage for charger detection
R2	VDRV	O	Charger current drive output
P2	BATON	I	Battery NTC pin for battery and its temperature sensing
P3	CHRLDO	O	CHRLDO output voltage
R8	AVDD28_RTC	O	RTC LDO output. Supply of RTC macro where backup battery can be added.
R7	AVSS28_RTC	GND	RTC ground
T6	XIN	IO	32K crystal connection port while using crystal to generate 32kHz clock
R6	XOUT	IO	32K crystal connection port while using crystal to generate 32kHz clock
T1	XOSC_EN	O	XOSC_EN control of RF chip
R3	ENBB	O	ENBB control of RF chip
M9	RTC32K_2V8	O	VRTC domain 32kHz clock output
P5	RTC32K_1V8_0	O	VIO18 domain 32kHz clock output
R4	RTC32K_1V8_1	O	VIO18 domain 32kHz clock output
R16	ISINK0	IO	ISINK channel 0
P15	ISINK1	IO	ISINK channel 1
N14	AVSS45_ISINK	GND	ISINK ground
T2	DVDD18_IO	PWR	Digital IO power
T3	DVDD18_DIG	O	VDIG18 output voltage
T5	DVSS18_IO	GND	Digital IO ground
F15	AU_FLYN	O	Flying capacitor bottom
G15	AU_FLYP	O	Flying capacitor top
H14	AU_REFN	GND	Audio reference ground
F13	AVSS18N_AUD	PWR	Audio -1.8V supply
G13	AVDD18_AUD	PWR	1.8V power supply of Audio
G14	AVSS18_AUD	GND	Audio DL ground
F16	SPK_P	O	Positive output of internal speaker amp
E16	SPK_N	O	Negative output of internal speaker amp
N15	AU_MICBIAS1	O	Microphone Bias 1
N16	AU_MICBIAS0	O	Microphone Bias 0
D14	AVDD45_SPK	PWR	Power supply of SPK
E14	AVSS45_SPK	GND	GND of internal speaker amp
M15	AU_VIN0_N	I	Microphone channel 0 negative input
M16	AU_VIN0_P	I	Microphone channel 0 positive input
L13	AU_VIN1_N	I	Microphone channel 1 negative input
K13	AU_VIN1_P	I	Microphone channel 1 positive input
L14	AU_VIN2_N	I	Microphone channel 2 negative input
K14	AU_VIN2_P	I	Microphone channel 2 positive input
H15	AU_HPL	O	Earphone left channel output
H16	AU_HPR	O	Earphone right channel output

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Ball	Symbol	I/O	Description
J12	CLK26M	I	26MHz clock input
J14	AU_HSN	O	Handset negative output
K15	AU_HSP	O	Handset positive output
M10	AUD_DAT_MISO	IO	Audio control interface
N8	AUD_DAT_MOSI	IO	Audio control interface
K12	AVSS28_AUD	GND	Audio UL ground
K16	AVDD28_AUD	PWR	2.8V supply of Audio UL
M8	AUD_CLK	I	Audio control interface

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2 Electrical Characteristics

2.1 Absolute Maximum Ratings over Operating Free-Air Temperature Range

Stresses beyond those listed in Table 2-1. Absolute maximum ratingsmay cause permanent damage to the device. These numbers are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 2-1. Absolute maximum ratings

Parameter	Conditions	Min.	Typical	Max.	Unit
Free-air temperature range		-40		85	°C
Storage temperature range		-65		150	°C
Battery Pin input voltage range				4.5	V
ESD robustness	HBM	2,000			V
Charger input withstand				30	V

2.2 Thermal Characteristic

Parameter	Conditions	Min.	Typical	Max.	Unit
Thermal resistance from junction to ambient	In free air		36.92[1]		°C/W

Note: The device is mounted on a 4-metal-layer PCB and modeled per JEDEC51-9 condition.

2.3 Pin Voltage Range

The table below lists operation rang voltages for all MT6328 I/O pins.

Table 2-2. Pin voltage range

Ball	Symbol	Voltage range	Unit
A1,B1	AVDD45_VSYS22	0 ~ 4.5	v
A2,B2	VSYS22	0 ~ 4.5	v
A3,B3	AVSS45_VSYS22	0	v
C3	VSYS22_FB	0	v
B4,C5,C4	AVDD45_VCORE1	0 ~ 4.5	v
A5,A6,B5	VCORE1	0 ~ 4.5	v

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Ball	Symbol	Voltage range	Unit
B6,C6,D6	AVSS45_VCORE1	0	V
C1	AVSS45_VCORE1_FB	0	V
C2	VCORE1_FB	0 ~ 4.5	V
A11,B10,B11,C10,D10	AVDD45_VPROC	0 ~ 4.5	V
A7,B7,B8,C7,D7	VPROC	0 ~ 4.5	V
A9,B9,C8,C9,D9	AVSS45_VPROC	0	V
B15	AVSS45_VPROC_FB	0	V
C16	VPROC_FB	0 ~ 4.5	V
B13,C13,D13	AVDD45_VLTE	0 ~ 4.5	V
A12,B12,C12	VLTE	0 ~ 4.5	V
C11,D11,D12	AVSS45_VLTE	0	V
E13	AVSS45_VLTE_FB	0	V
C14	VLTE_FB	0 ~ 4.5	V
A16	AVDD45_VPA	0 ~ 4.5	V
A15	VPA	0 ~ 4.5	V
A14	AVSS45_VPA	0	V
B14	VPA_FB	0 ~ 4.5	V
C15	AVDD45_SMPS	0 ~ 4.5	V
B16	AVSS45_SMPS	0	V
D5,E5,E6,E7,E8,E9, E10,E11,E12,F11,F12, G6,G7,G8,G9,G10,G11,G12,H6,H7, H8,H9,H10,H11,H12,J6,J7,J8,J9,J10,J11,K7,K8,K9,K10,K11,L7,L8,L9,L10,L11,L12	AVSS45_LDO	0	V
T13	AVDD45_LDO1	0 ~ 4.5	V
T8	AVDD45_LDO2	0 ~ 4.5	V
K1	AVDD45_LDO3	0 ~ 4.5	V
T11	AVDD45_LDO4	0 ~ 4.5	V
M2	AVDD45_LDO5	0 ~ 4.5	V
H3	AVDD22_LDO1	0 ~ 2.42	V
J2	AVDD22_LDO1	0 ~ 2.42	V
E1	AVDD22_LDO2	0 ~ 2.42	V
F1	AVDD22_LDO3	0 ~ 2.42	V
G1	AVDD22_LDO4	0 ~ 2.42	V
P9	VTCXO_0	0 ~ 4.5	V
T16	VTCXO_1	0 ~ 4.5	V
F10	VRF18_0	0 ~ 4.5	V
F9	VRF18_1	0 ~ 4.5	V
J1	VM	0 ~ 4.5	V

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Ball	Symbol	Voltage range	Unit
E4	VSRAM	0 ~ 1.98	V
H2	VCAMD	0 ~ 1.98	V
T14	VCAMA	0 ~ 4.5	V
E3	VCAMIO	0 ~ 4.5	V
H5	VCAMAF	0 ~ 4.5	V
F2	VIO18	0 ~ 4.5	V
K2	VIO28	0 ~ 4.5	V
K4	VMC	0 ~ 4.5	V
R9	VMCH	0 ~ 4.5	V
R10	VEMC_3V3	0 ~ 4.5	V
T15	VEFUSE	0 ~ 4.5	V
P11	VUSB33	0 ~ 4.5	V
R11	VSIM1	0 ~ 4.5	V
N11	VSIM2	0 ~ 4.5	V
F3	VCN18	0 ~ 4.5	V
R13	VCN28	0 ~ 4.5	V
R12	VCN33	0 ~ 4.5	V
R14	VAUD28	0 ~ 4.5	V
R15	VAUX18	0 ~ 4.5	V
H4	VGP1	0 ~ 4.5	V
J4	VIBR	0 ~ 3.3	V
E2	PWRKEY	0 ~ 4.5	V
D2	EXT_PMIC_EN	0 ~ 4.5	V
D3	RESETB	0 ~ 1.98	V
M7	WDTRSTB_IN	0 ~ 1.98	V
D4	PMU_TESTMODE	0 ~ 4.5	V
L4	VREF	0 ~ 1.32	V
L3	AVSS45_VREF	0	V
N5	SPI_MISO	0 ~ 1.98	V
L6	SPI_MOSI	0 ~ 1.98	V
K6	SPI_CLK	0 ~ 1.98	V
M6	SPI_CSN	0 ~ 1.98	V
N2	UVLO_VTH	0 ~ 3.3	V
N6	HOMEKEY	0 ~ 1.98	V
P4	FSOURCE	0 ~ 1.98	V
P8	SRCLKEN_IN0	0 ~ 1.98	V
R5	SRCLKEN_IN1	0 ~ 1.98	V

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Ball	Symbol	Voltage range	Unit
M12	AVDD18_AUXADC	0 ~ 1.98	v
M14	ACCDET	0 ~ 3.08	v
P14	AUXADC_VIN	0 ~ 1.98	v
N13	AVSS18_AUXADC	0	v
N3	BATSNS	0 ~ 4.5	v
N4	ISENSE	0 ~ 4.5	v
M4	VSYSSNS	0 ~ 4.5	v
N1	CHG_DP	0 ~ 4.5	v
M1	CHG_DM	0 ~ 4.5	v
D15	CS_P	0 ~ 0.1	v
E15	CS_N	0 ~ 0.1	v
J5	FCHR_ENB	0 ~ 4.5	v
P13	TREF	0 ~ 1.98	v
R1	VCDT	0 ~ 1.8	v
R2	VDRV	0 ~ 4.5	v
P2	BATON	0 ~ 4.5	v
P3	CHRLDO	0 ~ 3.08	v
R8	AVDD28_RTC	0~3.08	v
R7	AVSS28_RTC	0	v
T6	XIN	0 ~ 3.08	v
R6	XOUT	0 ~ 3.08	v
T1	XOSC_EN	0 ~ 3.08	v
R3	ENBB	0 ~ 1.98	v
M9	RTC32K_2V8	0 ~ 3.08	v
P5	RTC32K_1V8_0	0 ~ 1.98	v
R4	RTC32K_1V8_1	0 ~ 1.98	v
R16	ISINK0	0 ~ 4.5	v
P15	ISINK1	0 ~ 4.5	v
N14	AVSS45_ISINK	0	v
T2	DVDD18_IO	0 ~ 1.98	v
T3	DVDD18_DIG	0 ~ 1.98	v
T5	DVSS18_IO	0	v
F15	AU_FLYN	-1.98 ~ 0	v
G15	AU_FLYP	0 ~ 1.8	v
H14	AU_REFN	0	v
F13	AVSS18N_AUD	-1.98 ~ 0	v
G13	AVDD18_AUD	0 ~ 1.98	v

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Ball	Symbol	Voltage range	Unit
G14	AVSS18_AUD	0	V
F16	SPK_P	0 ~ 4.5	V
E16	SPK_N	0 ~ 4.5	V
N15	AU_MICBIAS1	0~3.08	V
N16	AU_MICBIAS0	0~3.08	V
D14	AVDD45_SPK	0 ~ 4.5	V
E14	AVSS45_SPK	0	V
M15	AU_VIN0_N	0~3.08	V
M16	AU_VIN0_P	0~3.08	V
L13	AU_VIN1_N	0~3.08	V
K13	AU_VIN1_P	0~3.08	V
L14	AU_VIN2_N	0~3.08	V
K14	AU_VIN2_P	0~3.08	V
H15	AU_HPL	-1.98 ~ 1.98	V
H16	AU_HPR	-1.98 ~ 1.98	V
J12	CLK26M	0 ~ 1.98	V
J14	AU_HSN	-1.98 ~ 1.98	V
K15	AU_HSP	-1.98 ~ 1.98	V
M10	AUD_DAT_MISO	0 ~ 1.98	V
N8	AUD_DAT_MOSI	0 ~ 1.98	V
K12	AVSS28_AUD	0	V
K16	AVDD28_AUD	0 ~ 3.08	V
M8	AUD_CLK	0 ~ 1.98	V

2.4 Recommended Operating Range

Table 2-3. Operation condition

Parameter	Conditions	Min.	Typical	Max.	Unit
Operating temperature range		-25		85	°C

2.5 Electrical Characteristics

VBAT = 2.5 ~ 4.5V, minimum loads applied on all outputs, unless otherwise noted.
Typical values are at T_A = 25°C.

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Table 2-4. General electrical specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Operation Ground Current					
Standby	Low-power mode		250	300	µA
Power down leakage current with 32K XTAL	VBAT=4.5V, Temp=-40°C~85°C		55	100	uA
Power down leakage current without 32K XTAL	VBAT=4.5V, Temp=-40°C ~85°C		70	115	uA
Under Voltage (UV)					
Under voltage falling threshold 1	Programmable, 50mV steps.	2.5	2.6	2.9	V
Threshold voltage accuracy		-50		+50	mV
Under voltage rising threshold	UV_SEL[4:0] = xxxxx (w/o charger)	2.95	3.0	3.05	V
Under voltage rising threshold w/o power path	UV_SEL[4:0] = xxxxx (w/i charger)	2.75	2.8	2.85	V
Under voltage rising threshold with power path	UV_SEL[4:0] = xxxxx (w/i charger)	2.95	3.0	3.05	V
Reset Generator					
Output high		VIO-0.4			V
Output low				0.2	V
Output current (Ioh)	Vo > VIO-0.4V		1		mA
Delay Time from VMC turn on to RESETB release		32	40	48	ms
Interrupt					
Output high		VIO-0.4			V
Output low				0.2	V
PWRKEY					
High voltage		0.7*VBAT			V
Low voltage				0.3*VBAT	V
De-bounce time		26	32	38	ms
Control Input Voltage					
Control input high (HOMEKEY, SPI, SRCLKEN related)		0.7*VIO			V
Control input low (HOMEKEY, SPI, SRCLKEN related)				0.3*VIO	V
Thermal Shut-down					
PMIC shut-down threshold			150		degree
Shut-down release threshold			110		degree

2.6 Regulator Output

Table 2-5. Buck specifications

Parameter	Conditions	Min.	Typical	Max.	Unit

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Parameter	Conditions	Min.	Typical	Max.	Unit
Buck – VPROC					
Turn-on overshoot	No load			10	%
Short current		Imax*1.2		Imax*2.5	
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=0.85V, L_DCR=35mohm I_Load=100mA		83		%
	Vbat=3.8V, Vout=1.05V, L_DCR=35mohm I_Load=500mA		83		%
	Vbat=3.8V, Vout=1.15V, L_DCR=35mohm I_Load=2.5A		83		%
	Vbat=3.8V, Vout=1.15V, L_DCR=35mohm I_Load=4A		80		%
	Vbat=3.8V, Vout=1.15V, L_DCR=35mohm I_Load=5A		77		%
Soft start	No load			1	ms
Output Ripple Voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVpp
Load transient(PWM)	Vbat=3.8V IOUT = 1.5A to 4A (slew rate=2.5A/us)	-3.5		+3.5	%
DC Accuracy (Included Line/Load regulation @PWM)	VBAT=2.8V to 4.5V I_Load=10mA to Imax	-1		+1	%
DC Accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 4.5V I_Load=0~10mA	-2		+3	%
Buck – VCORE1					
Turn-on overshoot	No load			10	%
Short current		Imax*1.2		Imax*2.5	
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=1.05V, L_DCR=40mohm I_Load=100mA		83		%
	Vbat=3.8V, Vout=1.15V, L_DCR=40mohm I_Load=800mA		85		%
	Vbat=3.8V, Vout=1.25V, L_DCR=40mohm I_Load=2.6A		70		%
	Vbat=3.8V, Vout=1.25V L_DCR=40mohm I_Load=3.2A		60		%
Soft start	No load			1	ms
Output Ripple Voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax			20	mVpp

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Parameter	Conditions	Min.	Typical	Max.	Unit
	20MHz measurement BW				
Load transient(PWM)	Vbat=3.8V IOUT = 1.0A to 2.0A (slew rate=1A/us)	-3.5		+3.5	%
DC Accuracy (Included Line/Load regulation @PWM)	VBAT=2.8V to 4.5V I_Load=10mA to Imax	-1		+1	%
DC Accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 4.5V I_Load=0~10mA	-2		+3	%
Buck – VLTE					
Turn-on overshoot	No load			10	%
Short current		Imax*1.2		Imax*2.5	
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=0.85V, L_DCR=40mohm I_Load=100mA		83		%
	Vbat=3.8V, Vout=1.05V, L_DCR=40mohm I_Load=800mA		85		%
	Vbat=3.8V, Vout=1.05V L_DCR=40mohm I_Load=2.2A		75		%
	Vbat=3.8V, Vout=1.05V L_DCR=40mohm I_Load=2.6A		70		%
Soft start	No load			1	ms
Output Ripple Voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVpp
Load transient(PWM)	Vbat=3.8V IOUT = 1.0A to 2.5A (slew rate=1.5A/us)	-3.5		+3.5	%
DC Accuracy (Included Line/Load regulation @PWM)	VBAT=2.8V to 4.5V I_Load=10mA to Imax	-1		+1	%
DC Accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 4.5V I_Load=0~10mA	-2		+3	%
Buck – VSYS22					
Turn-on overshoot	No load			10	%
Short current		Imax*1.2		Imax*3	
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, L_DCR=40mohm I_Load=50mA		87		%
	Vbat=3.8V, L_DCR=40mohm I_Load=500mA		88		%
	Vbat=3.8V,		87		%

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Parameter	Conditions	Min.	Typical	Max.	Unit
	L_DCR=40mohm I_Load=1000mA				
Soft start	No load			1	ms
Output Ripple Voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVpp
Load transient(PWM)	Vbat=3.8V IOUT = 1.0A to 2.0A (slew rate=1000mA/us)	-3.5		+3.5	%
DC Accuracy (Included Line/Load regulation @PWM)	VBAT=2.8V to 4.5V I_Load=10mA to Imax	-3		+3	%
DC Accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 4.5V I_Load=1~500mA	-3		+3	%
Buck – VPA					
Turn-on overshoot	No load			10	%
Short current				Imax*5	
Temperature Coefficient	Vbat=3.8V I_Load=0.5*Imax Vo=1.8V	-100		+100	ppm/C
Efficiency	Vbat=3.8V, L_DCR=110 mohm I_Load=80mA Vo=1.2V		82		%
	Vbat=3.8V, L_DCR=110 mohm I_Load=180mA Vo=2.4V		88		%
	Vbat=3.8V, L_DCR=110mohm I_Load=280mA Vo=3.4V		95		%
Soft start	No load			200	us
Output Ripple Voltage (PWM)	Vbat=3.8V Vo=1.8V I_Load=0.5*Imax 20MHz measurement BW			30	mVpp
DC Accuracy (Included Line/Load regulation @PWM)	VBAT=2.8V to 4.5V Vo=1.7V I_Load=10mA~360mA	-5		+5	%
No load quiescent current (PFM)	VBAT=3.8V Vo=0.5V I_Load=0A		150		uA

Table 2-6. LDO specifications

Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
All test condition	VBAT range	LDO output voltage ≦ 2.1V			2.5	V

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Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
		LDO output voltage > 2.1V	Output Voltage +0.35V		4.5	V
Droup out voltage	All LDOs				350	mV
Line/ Load regulation	VTCXO_0, VTCXO_1	1. Iout= 0~Imax 2. VBAT range 3. Capacitor range= Min~max 4. TA= -25°C ~+65°C	-100		+100	mV
	VRF18_0 , VRF18_1		-75		+75	mV
	VCAMA		-3		+3	%
	VSRAM, VM, VSIM1, VSIM2, VAUX18, VAUD28, VCAMD		-1		+1	%
	ALDO and DLDO		-5		+5	%
	VRTC		2			V
	DVDD18_DIG		-10		10	%
	ALDO and DLDO low power mode	1. Iout= 0~0.05*Imax 2. VBAT range 3. Capacitor range= Min~max 4. TA= -25°C ~+65°C	-5		+5	%
Temperature coefficient	ALDO and DLDO	TA= -25°C~+65°C	-100		+100	ppm/C
Load transient response	VMCH, VEMC33	1. Iout= 0.1mA~50mA (slew rate= 50mA/us) 2. VBAT range 3. Capacitor range= Min~max 4. TA= -25°C ~+65°C	-5		+5	%
	VCAMA	1. Iout= 1mA~Imax (slew rate= 15mA/us) 2. VBAT range 3. Capacitor range= Min~max 4. TA= -25°C ~+65°C	-3		+3	%
	VRF18_0, VRF18_1	1. Iout= 100mA~200mA (slew rate= 100mA/us) 2. VBAT range 3. Capacitor range= Min~max 4. TA= -25°C ~+65°C	-5		+5	%

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Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
	VCN33	1. Iout= 1mA~350mA (slew rate= 70mA/us) 2. VBAT range 3. Capacitor range= Min~max 4. TA= -25°C ~+65°C	-6		+6	%
	VSRAM	1. Iout= 1mA~150mA (slew rate= 150mA/us) 2. VBAT range 3. Capacitor range= Min~max 4. TA= -25°C~+65°C	-4		+4	%
	VM	1. Iout= 0.01mA~600mA (slew rate= 600mA/us) 2. VBAT range 3. Capacitor range= Min~max 4. TA= -25°C~+65°C	-4		+4	%
	VGP1	1. Iout= 0.01mA~150mA (slew rate= 50mA/us) 2. VBAT range 3. Capacitor range= Min~max 4. TA= -25°C~+65°C	-4		+4	%
	ALDO and DLDO	1. Iout= 1mA~Imax (slew rate= 15mA/us) 2. VBAT range 3. Capacitor range= Min~max 4. TA= -25°C~+65°C	-5		+5	%
Turn-on rise time	ALDO and DLDO	1. Iout= 0mA 2. VBAT range 3. Capacitor range= min 4. TA= +25°C			300	us
Turn-on overshoot	ALDO and DLDO	1. Iout= 0mA 2. VBAT range 3. Capacitor range= min 4. TA= +25°C			+10	%
Output noise	ALDO	1. Freq= 10Hz to 80kHz 2. Iout= 0.01*Imax/ 0.5*Imax		90		uVrms

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Parameter	Type	Conditions	Min.	Typ.	Max.	Unit
	DLDO	3. VBAT range 4. Capacitor range= min 5. TA= +25°C		500		uVrms
PSRR	ALDO	1. Freq= 217Hz to 3kHz 2. Iout= 0.01*Imax/ 0.5*Imax 3. VBAT range 4. Capacitor range= min 5. TA= +25°C		65		dB
	DLDO	1. Freq= 217Hz 2. Iout= 0.01*Imax/ 0.5*Imax 3. VBAT range 4. Capacitor range= min 5. TA= +25°C		40		dB
Short current	ALDO and DLDO	VBAT range	Imax* 1.2		Imax* 5	
Normal mode quiescent current	VCAMA	1. Iout= 0mA 2. VBAT range 3. Capacitor range= min 4. TA= +25°C			300	uA
	VMCH/VEMC33/ VRF18_0/VRF18_1				100	uA
	VSRAM/VCN33/VM				200	uA
	DIG18				5	uA
	Other LDO				55	uA
Low power mode quiescent current	VMCH				15	uA
	ALDO and DLDO				10	uA

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2.7 Driver

Table 2-7. Driver specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
ISINK					
ISINK LED sink current	ISINK_SEL = 000	3.6	4	4.4	mA
	ISINK_SEL = 001	7.2	8	8.8	mA
	ISINK_SEL = 010	10.8	12	13.2	mA
	ISINK_SEL = 011	14.4	16	17.6	mA
	ISINK_SEL = 100	18	20	22	mA
	ISINK_SEL = 101	21.6	24	26.4	mA
ISINK dropout voltage	4 ~ 24mA VISINK drop		150	250	mV
ISINK rise/fall time	VISINK > 0.3V			3.33	uS
VIBR					
Output voltage	VIBR_SEL = 000	1.1	1.2	1.3	V
	VIBR_SEL = 001	1.2	1.3	1.4	V
	VIBR_SEL = 010	1.4	1.5	1.6	V
	VIBR_SEL = 011	1.7	1.8	1.9	V
	VIBR_SEL = 100	2.35	2.5	2.65	V
	VIBR_SEL = 101	2.65	2.8	2.95	V
	VIBR_SEL = 110	2.85	3.0	3.15	V
	VIBR_SEL = 111	3.1	3.3	3.5	V
Output current			100		mA

2.8 Class AB/D Audio Amplifier

Table 2-8. Class AB/D audio amplifier specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Class AB Audio Amplifier					
RMS power	8Ω load, VBAT = 4.2V THD + N = 1%		890		mW
	8Ω load, VBAT = 3.8V THD + N = 1%		700		mW
	8Ω load, VBAT = 3.4V THD + N = 1%		500		mW
	8Ω load, VBAT = 4.2V THD + N = 10%		1100		mW
	8Ω load, VBAT = 3.8V THD + N = 10%		850		mW
	8Ω load, VBAT = 3.4V THD + N = 10%		600		mW
THD+N	1kHz, Po = 0.5Wrms, VBAT = 4.2V		0.01	0.03	%
	1kHz, Po = 0.4Wrms, VBAT = 3.8V		0.01	0.03	%

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Parameter	Conditions	Min.	Typ.	Max.	Unit
	1kHz, Po = 0.3Wrms, VBAT = 3.4V		0.01	0.03	%
PSRR	217Hz, Vin = 200mVpk-pk Input AC to ground, VBAT = 4.2V		80		dB
	217Hz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		80		dB
	217Hz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.4V		80		dB
	1kHz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		80		dB
	4kHz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		80		dB
	20kHz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		80		dB
Noise level	VBAT = 4.2V, 12dB gain 8Ω, A-weighted		30		μV
	VBAT = 3.4V, 12dB gain 8Ω, A-weighted		30		uV
	VBAT = 4.2V, 0dB gain 8Ω, A-weighted		10		μV
	VBAT = 3.4V, 0dB gain 8Ω, A-weighted		10		uV
	VBAT = 4.2V, -6dB gain 8Ω, A-weighted		6		μV
	VBAT = 3.4V, -6dB gain 8Ω, A-weighted		6		uV
Gain adjustment		6		15	dB
Gain adjustment steps			1		dB
Quiescent current	No load, VBAT=4.2V		5		mA
	No load, VBAT=3.8V		5		mA
	No load, VBAT=3.4V		5		mA
DC offset	VBAT = 4.2V, 12dB gain		5		mV
	VBAT = 3.8V, 12dB gain		5		mV
	VBAT = 3.4V, 12dB gain		5		mV
	VBAT = 4.2V, 0dB gain		1		mV
	VBAT = 3.8V, 0dB gain		1		mV
	VBAT = 3.4V, 0dB gain		1		mV
	VBAT = 4.2V, -6dB gain		1	5	mV
	VBAT = 3.8V, -6dB gain		1	5	mV
	VBAT = 3.4V, -6dB gain		1	5	mV
Class D Audio Amplifier					
RMS power	8Ω load, VBAT = 4.2V THD + N = 1%		900		mW

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Parameter	Conditions	Min.	Typ.	Max.	Unit
	8Ω load, VBAT = 3.8V THD + N = 1%		700		mW
	8Ω load, VBAT = 3.4V THD + N = 1%		500		mW
	8Ω load, VBAT = 4.2V THD + N = 10%		1100		mW
	8Ω load, VBAT = 3.8V THD + N = 10%		850		mW
	8Ω load, VBAT = 3.4V THD + N = 10%		600		mW
THD+N	1kHz, Po = 0.5Wrms, VBAT = 4.2V		0.02	0.16	%
	1kHz, Po = 0.4Wrms, VBAT = 3.8V		0.02	0.16	%
	1kHz, Po = 0.3Wrms, VBAT = 3.4V		0.02	0.16	%
PSRR	217Hz, Vin = 200mVpk-pk Input AC to ground, VBAT = 4.2V		80		dB
	217Hz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		80		dB
	217Hz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.4V		80		dB
	1kHz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		80		dB
	4kHz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		80		dB
	20kHz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		80		dB
Noise level	VBAT = 4.2V, 12dB gain 8Ω, A-weighted		60		µV
	VBAT = 3.4V, 12dB gain 8Ω, A-weighted		60		uV
	VBAT = 4.2V, 0dB gain 8Ω, A-weighted		25		µV
	VBAT = 3.4V, 0dB gain 8Ω, A-weighted		25		uV
Efficiency	VBAT = 4.2V 0.8W, 8Ω with 68uH, 1kHz		85		%
	VBAT = 4.2V 0.5W, 8Ω with 68uH, 1kHz		85		%
	VBAT = 3.8V 0.5W, 8Ω with 68uH, 1kHz		85		%
	VBAT = 3.4V 0.5W, 8Ω with 68uH, 1kHz		85		%

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Parameter	Conditions	Min.	Typ.	Max.	Unit
Gain adjustment		6		15	dB
Gain adjustment steps			1		dB
Quiescent current	No load, VBAT=4.2V		5		mA
	No load, VBAT=3.8V		5		mA
	No load, VBAT=3.4V		5		mA
DC offset	VBAT = 4.2V, 12dB gain			5	mV
	VBAT = 3.8V, 12dB gain			5	mV
	VBAT = 3.4V, 12dB gain			5	mV
	VBAT = 4.2V, 0dB gain		1		mV
	VBAT = 3.8V, 0dB gain		1		mV
	VBAT = 3.4V, 0dB gain		1		mV

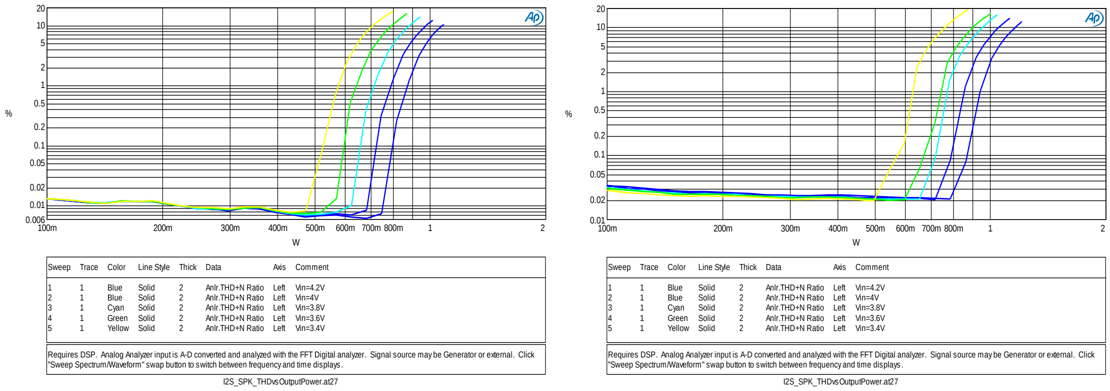

Figure 2-1. THD+N v.s. output power (Class AB/D, VBAT=4.2/3.8/3.4V, gain=12dB)

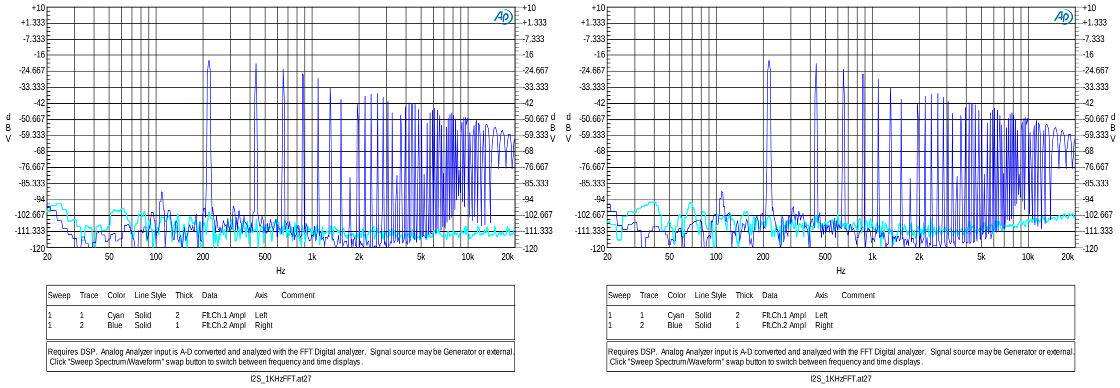

Figure 2-2. PSRR with 217Hz TDMA noise (Class AB/D, VBAT=3.8V, gain=12dB)

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2.9 Audio CODEC

Table 2-9. Audio downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
DAC to Audio Buffer Output (single-ended output, AU_HPL/R; R_{LOAD} = 32) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, Gain = +0dB, 24bit audio data (default)					
P_{OUT}	Maximum output power @<0.1% THD		25		mW
SNR (1)	Signal to noise ratio (A-weighted)		100		dB(A)
THD	Total Harmonic distortion (THD) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		 -86 -88 -86		dB
THD+N	THD plus noise (THD+N) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		 -84 -86 -84		dB
NF_{OUT}	Output noise floor (A-weighted)		4		µVrms (A)
R_{LOAD}	Output resistor load (headphone)	16	32		Ω
C_{LOAD}	Output capacitor load			250	pF
$APGR_{DL}$	Analog programmable gain range	-10		8	dB
$APGS_{DL}$	Analog programmable gain step		1		dB
XT_{LR}	L/R channel crosstalk @1kHz		-90		dB
PSRR	Power supply rejection ratio (From AVDD18_AUD to AU_HPL/R)		90		dB
DAC to Audio Buffer Output (single-ended output, AU_HPL/R; R_{LOAD} = 16) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, Gain = +0dB, 24bit audio data (default)					
P_{OUT}	Maximum output power @<0.1% THD		35		mW
SNR (1)	Signal to noise ratio (A-weighted)		100		dB(A)
THD	Total Harmonic distortion (THD) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		 -84 -88 -88		dB
THD+N	THD plus noise (THD+N) @P_{OUT} = 2mW @P_{OUT} = 10mW @P_{OUT} = 22.5mW		 -81 -86 -86		dB
NF_{OUT}	Output noise floor (A-weighted)		4		µVrms (A)

Note 1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer

Note 2: The output voltage range of both audio and voice buffer outputs are within [AVSS18N_AUD, AVDD18_AUD]

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Symbol	Parameter	Min.	Typ.	Max.	Unit
DAC to Voice Buffer Output (differential outputs, AU_HSP/N; R_{LOAD} = 32) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, Gain = +0dB, 24bit audio data (default)					
P_{OUT}	Maximum output power @<1% THD		100		mW
SNR (1)	Signal to noise ratio (A-weighted)		-104		dB(A)
THD	Total Harmonic distortion (THD) @P_{OUT} = 10mW @P_{OUT} = 50mW		 -87 -88		dB
THD+N	THD plus noise (THD+N) @P_{OUT} = 10mW @P_{OUT} = 50mW		 -85 -86		dB
NF_{OUT}	Output noise floor (A-weighted)		5		µVrms (A)
R_{LOAD}	Output resistor load (headphone)	16	32		Ω
C_{LOAD}	Output capacitor load			250	pF
$APGR_{DL}$	Analog programmable gain range	-10		8	dB
$APGS_{DL}$	Analog programmable gain step		1		dB
PSRR	Power supply rejection ratio (From AVDD18_AUD to AU_HSP/N)		90		dB
DAC to Voice Buffer Output (differential outputs, AU_HSP/N; R_{LOAD} =16) Temp = 25deg, 1kHz sinusoid signal, $F_{S,DL}$ = 48kHz, Gain = +0dB, 24bit audio data (default)					
P_{OUT}	Maximum output power @<1% THD		130		mW
SNR (1)	Signal to noise ratio (A-weighted)		-104		dB(A)
THD	Total harmonic distortion (THD) @P_{OUT} = 20mW @P_{OUT} = 100mW		 -87 -88		dB
THD+N	THD Plus noise (THD+N) @P_{OUT} = 20mW @P_{OUT} = 100mW		 -85 -86		dB
NF_{OUT}	Output noise floor (A-weighted)		5		µVrms (A)

Note 1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer

Note 2: The output voltage range of both audio and voice buffer outputs are within [AVSS18N_AUD, AVDD18_AUD]

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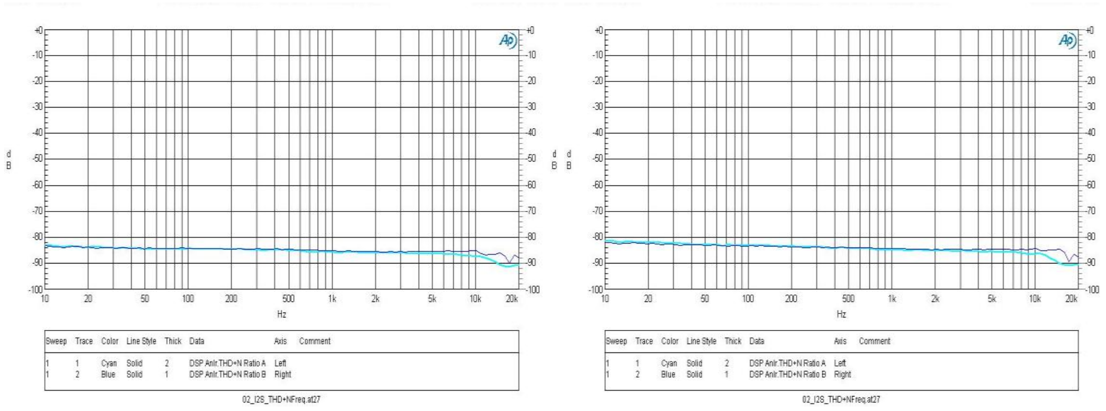
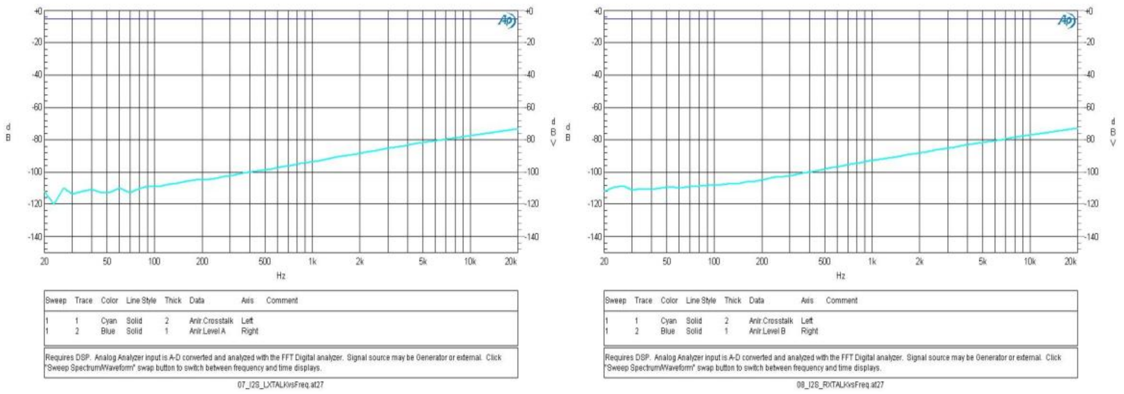


(a) P_{OUT}=10mW (b) P_{OUT}=22.5mW

Figure 2-3. Audio path THD+N v.s. frequency



(a) XtalkRtoL (b) XtalkLtoR

Figure 2-4. Audio path Xtalk v.s. frequency @P_{OUT}=10mW

Table 2-10. Audio uplink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Analogue Input Paths to ADC (differential) DCC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 0dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		98		dB
N_{IN}	Input-referred noise		16		µVrms
THD	Total Harmonic Distortion (THD) @0dBV input (-3dBFS)		-89		dB
THD+N	THD plus noise (THD+N) @0dBV input (-3dBFS)		-86		dB
	THD plus noise (THD+N) @-60dBV input (-63dBFS)		-36		dB
Analogue Input Paths to ADC (differential) DCC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 18dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		89		dB

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Symbol	Parameter	Min.	Typ.	Max.	Unit
N_{IN}	Input-referred noise		6.3		µVrms
THD	Total Harmonic Distortion (THD) @-18dBV input (-3dBFS)		-89		dB
THD+N	THD plus noise (THD+N) @-18dBV input (-3dBFS)		-84		dB
	THD plus noise (THD+N) @-78dBV input (-63dBFS)		-26		dB

Symbol	Parameter	Min.	Typ.	Max.	Unit
Analogue Input Paths to ADC (differential) ACC mode Temp = 25deg, 1kHz sinusoid signal, $F_{S,UL}$ = 48kHz, PGA_{UL} gain = 0dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		99		dB
N_{IN}	Input-referred noise		14		µVrms
THD	Total Harmonic Distortion (THD) @0dBV input (-3dBFS)		-87		dB
THD+N	THD plus noise (THD+N) @0dBV input (-3dBFS)		-85		dB
	THD plus noise (THD+N) @-60dBV input (-63dBFS)		-37		dB
Analogue Input Paths to ADC (differential) ACC mode Temp = 25deg, 1kHz sinusoid signal, FS,UL = 48kHz, PGAUL gain = 18dB, 16bit audio data (A-weighted)					
SNR*1	Signal to noise ratio		92		dB
N_{IN}	Input-referred noise		4.2		µVrms
THD	Total Harmonic Distortion (THD) @-18dBV input (-3dBFS)		-87		dB
THD+N	THD plus noise (THD+N) @-18dBV input (-3dBFS)		-84		dB
	THD plus noise (THD+N) @-78dBV input (-63dBFS)		-29		dB

Note 1: Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured w/i A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer

Note 2: The input voltage range of AU_VIN0, AU_VIN1, and AU_VIN2 are within [AVDD28_AUD, AVSS28_AUD], and suggesting maximum input swing $V_{pp} \le 1V_{rms}$ (0 dBV) @ PGA_{UL} gain = 0dB

General					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
$APGR_{UL}$	Uplink Analog Programmable Gain Range	0		24	dB
$APGS_{UL}$	Uplink Analog Programmable Gain Step		6		dB
CMRR	Common-mode Rejection Ratio @-18dBV, 1kHz sinusoid signal to both pins of an input configured differentially	40	76		dB
$XT_{Internal}$	ULL-to-ULR Channel Separation @ one input terminated with -18dBV, 1KHz sinusoid signal. Measure digital output of terminated channel	60	100		dB
XT_{DL2UL}	DL-to-UL Channel Separation @ 0dBV, 1kHz Rx path with RLOAD = 32	60	101		dB
PSRR	217Hz @ 200 mVpp square wave imposed on power. Measure digital output		-70		dB
	1kHz @ 200 mVpp square wave imposed on power. Measure digital output		-70		dB
	10kHz @ 200 mVpp square wave imposed on power.		-70		dB

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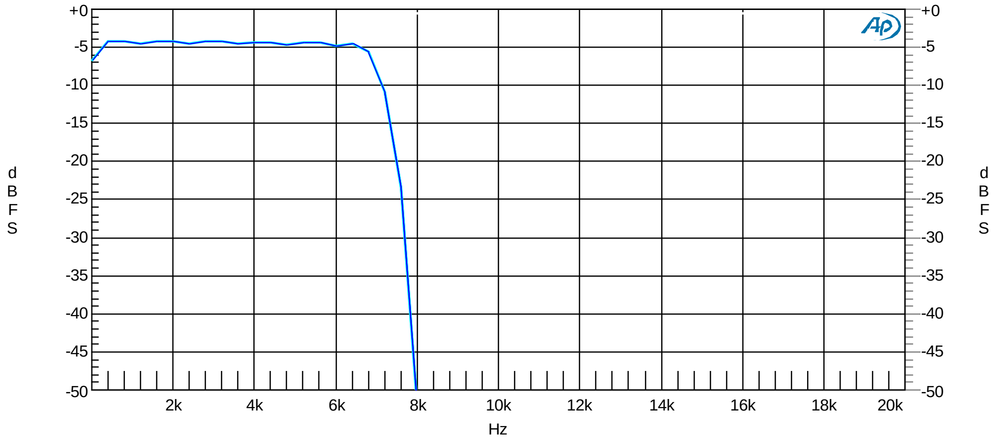
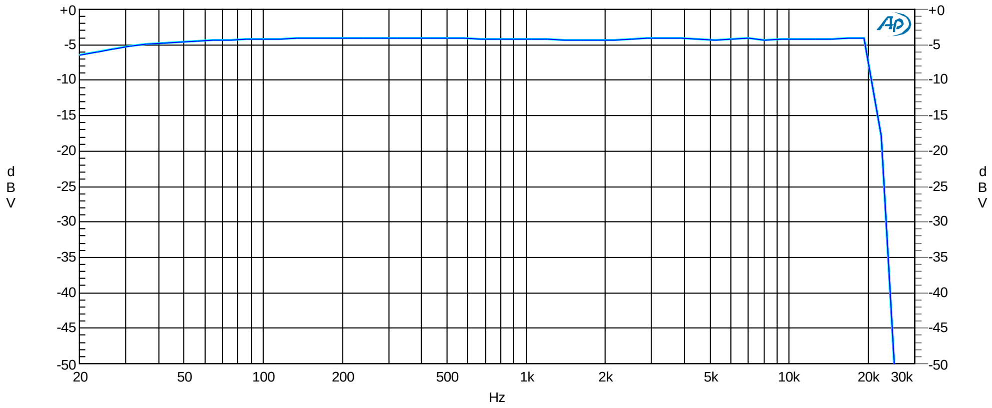
General					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
	Measure digital output				
$F_{S,UL}$	Audio Uplink Sampling Rate 8, 16, 32, and 48KHz	8		48	KHz



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	2	DSP Anlr.Level A	Left	
1	2	Blue	Solid	1	DSP Anlr.Level B	Right	

07_I2S_out_sweep_BW.at27

Figure 2-5. Frequency response (16kHz)



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	2	DSP Anlr.Level A	Left	
1	2	Blue	Solid	1	DSP Anlr.Level B	Right	

Requires DSP. Analog Analyzer input is A-D converted and analyzed with the FFT Digital analyzer. Signal source may be Generator or external.
Click "Sweep Spectrum/Waveform" swap button to switch between frequency and time displays.

07_I2S_out_sweep_BW.at27

Figure 2-6. Frequency response (48kHz)

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Digital MIC					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
DCLK	DMIC clock frequency		3.25/1.62		MHz
DTY	DMIC clock duty cycle	40		60	%
DCRT	DMIC clock rise time (MaxCL = 65p)			10	ns
DCFT	DMIC clock fall time (MaxCL = 65p)			10	ns

Table 2-11. MICBIAS specifications

Microphone Bias (MICBIAS) Temp = 25deg, 1μF capacitor on MICBIAS					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{OUT}	Microphone Bias Voltage	1.7		2.5	V
V_{OUT} Step	Bias Voltage Output Step Size 1.7~2.1 2.3~2.5		0.1		V
I_{OUT}	Maximum Output Current (Two MICBIAS loads total)			3	mA
N_{OUT}	Output Integrated Noise (20~20KHz A-weighted) with 1μF cap.		3.9		μVrms
PSRR	217Hz @ 200 mVpp square wave imposed on VBAT. Measure MICBIAS output		-100		dB
	1kHz @ 200 mVpp square wave imposed on VBAT. Measure MICBIAS output		-100		dB
	10kHz @ 200 mVpp square wave imposed on VBAT. Measure MICBIAS output		-95		dB
$C_{LOAD,MIC}$	Output Capacitor Load on MICBIAS	0.1		22	μF

Table 2-12. ACCDET specifications

Accessory Detection (ACCDET)					
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
-	*1: Load impedance detection range (ACCDET) by 1& 1.5kΩ (1%) MICBIAS resistors *2: Note the characteristics assume no other component is connected to ACCDET *3: Note the key detection voltage will be normalized automatic. For different MICBIAS setting , the same key (resistance is the same)is pressed , read voltage (key pressed) value will be similar				
-	4 pole Microphone Detection	2K		14K	Ohm
-	Microphone impedance detection after 4-pole microphone plugged-in				
-	MICD_LVL[0]: Down key	400		620	Ohm
-	MICD_LVL[1]: Up key	150		320	Ohm
	MICD_LVL[2]: Hook key	0		100	Ohm

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2.10 Battery Charger

Table 2-13. Charger specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
CHRIN(or called VBUS in ref. schematic) operating voltage		4.3	5	10.5	V
OTG B-Valid detection		0.8	2.4	4	V
VCDT detection threshold	VCDT_VTHL[3:0] = 0000 ~ 1111	4.3		10.5	V
HV adaptive current @ pre_charge	CHRIN switch threshold (300mA => 70mA)		7		V
	CHRIN switch threshold (70mA => 300mA)		6		V
VBAT CC voltage accuracy	Programmable: 3.3~3.45, 50mV steps	-50		+50	mV
VBAT CV voltage accuracy	Programmable: 3.5~4.4 V	-30		+30	mV
VBAT OV voltage accuracy	Programmable: 3.9~4.5 V	-30		+30	mV
CC mode charging current accuracy	Programmable:500 ~2000 mA (Rsense=56mohm)	-10		+10	%
	Programmable:300 ~500 mA (Rsense=56mohm)	-15		+15	%

2.11 BC1.x

Table 2-14. BC1.x specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
BC11 charging port detection (Pre-CC current)	Standard down-stream port	35	70	94	mA
	Standard charging down-stream port	35	70	94	mA
	DP, DM short	210	300	390	mA
BC11 characteristics	DP, DM floating	210	300	390	mA
	IPU_DP, IPU_DM	7	9.6	13	uA
	IPD_DP, IPD_DM	50	96	150	uA
	VSRC on DP, DM	500	630	700	mV
	Current pulse value under 2.2V		70		mA
	Current pulse period under 2.2V		550		ms
	OSC1M, timer		5		min

2.12 Down Load Without Battery

Table 2-15. Download without battery specifications

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Parameter	Conditions	Min.	Typ.	Max.	Unit
USBDL	Duration		32.0		s
	Current		450		mA

2.13 AUXADC

Table 2-16. AUXADC specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply voltage		-	1.8	-	V
Resolution	Channel 0,1,7	-	-	15	Bits
	Others	-	-	12	Bits
Analog-input bandwidth			0.5K		Hz
Sample rate			1K		Hz
Offset error	Relative to full-scale	-1	-	+1	%
Gain error	Relative to full-scale	-1	-	+1	%
INL	15-bit output		2		LSB
DNL	15-bit output		2		LSB

2.14 Fuel Gauge

Table 2-17. Fuel gauge specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
FG current characteristics	Output resolution		16		Bit
	Conversion time		1/16		s
	Over-sampling ratio	2^11		2^18	
ADC characteristics	Input voltage range	-60		60	mV
	Supply		2.8		V
	Current		40		uA
	Gain error	-2		2	%
	Accuracy		0.03		%

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3 Functional Descriptions

3.1 General Descriptions

MT6328 is a fully integrated PMIC target for smart phone power provider. Figure 3-1 is the block diagram of MT6328 PMIC.

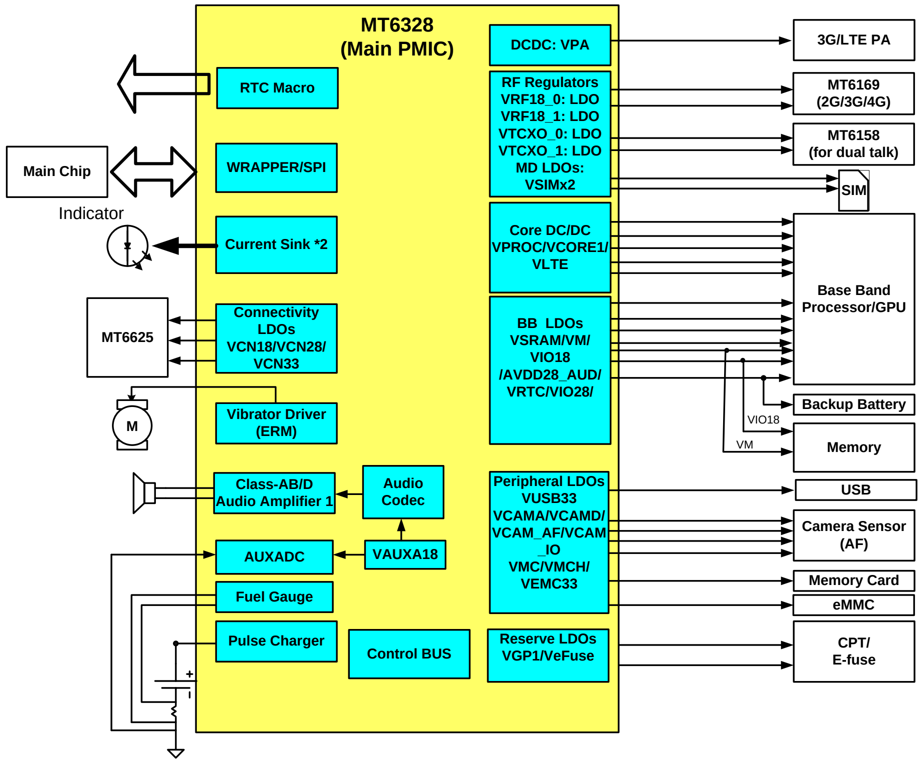

Figure 3-1. MT6328 block diagram

3.2 PMIC Functional Blocks

MT6328 manages the power supply of baseband processor, SIM cards, camera, vibrator, etc. MT6328 includes the following analog functions for use on smart phone platforms.

- LDO and BUCK: Provides regulated lower output voltage level from Li-Ion battery
- Current sink (ISINK) driver: Sink current for indicator
- Vibrator driver: Provides regulated power for vibrator.
- AUXADC: 15 bits of analog to digital converter for thermal/accessory detection monitor and measurement
- Controller: Generates power-on/off sequence, system reset and exceptional handling function

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- Charger controller: Controls/Protects battery charging procedure
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC
- Fuel gauge: Supports accurate battery capacity monitor

More detailed descriptions of each sub-block are explained in the following sections.

3.2.1 Power-On/Off Sequence

PMIC handles the power-on and power-off of the handset. If the battery voltage is neither in the UVLO state (VBAT ≥ UVLO_VTHH) nor in the thermal condition, there are 3 methods to power on the handset system.

1) Pulling PWRKEY low (User presses PWRKEY.)
2) Setting BBWAKEUP to high
3) Valid charger plug-in

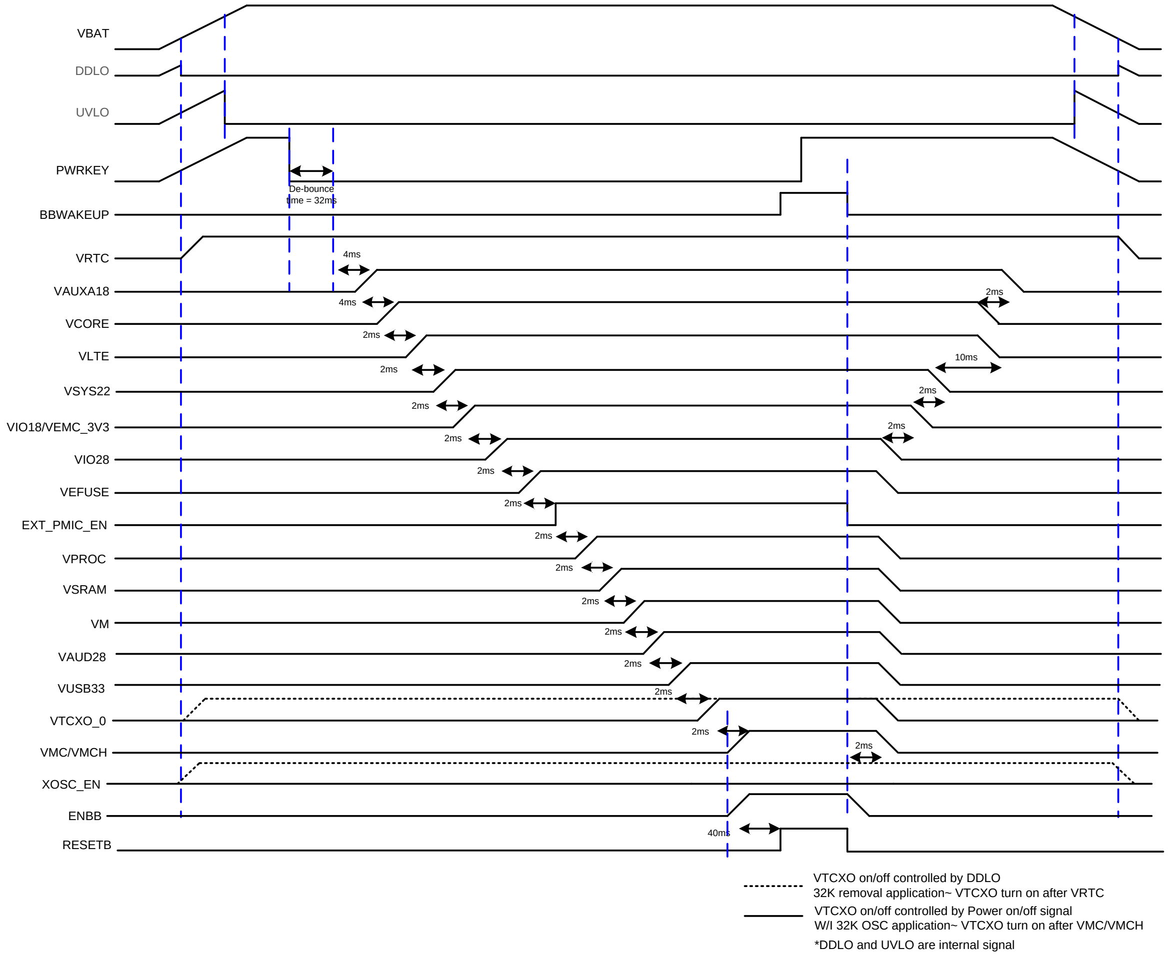

Figure 3-2. Power-on/off control sequence with XTAL by pressing PWRKEY

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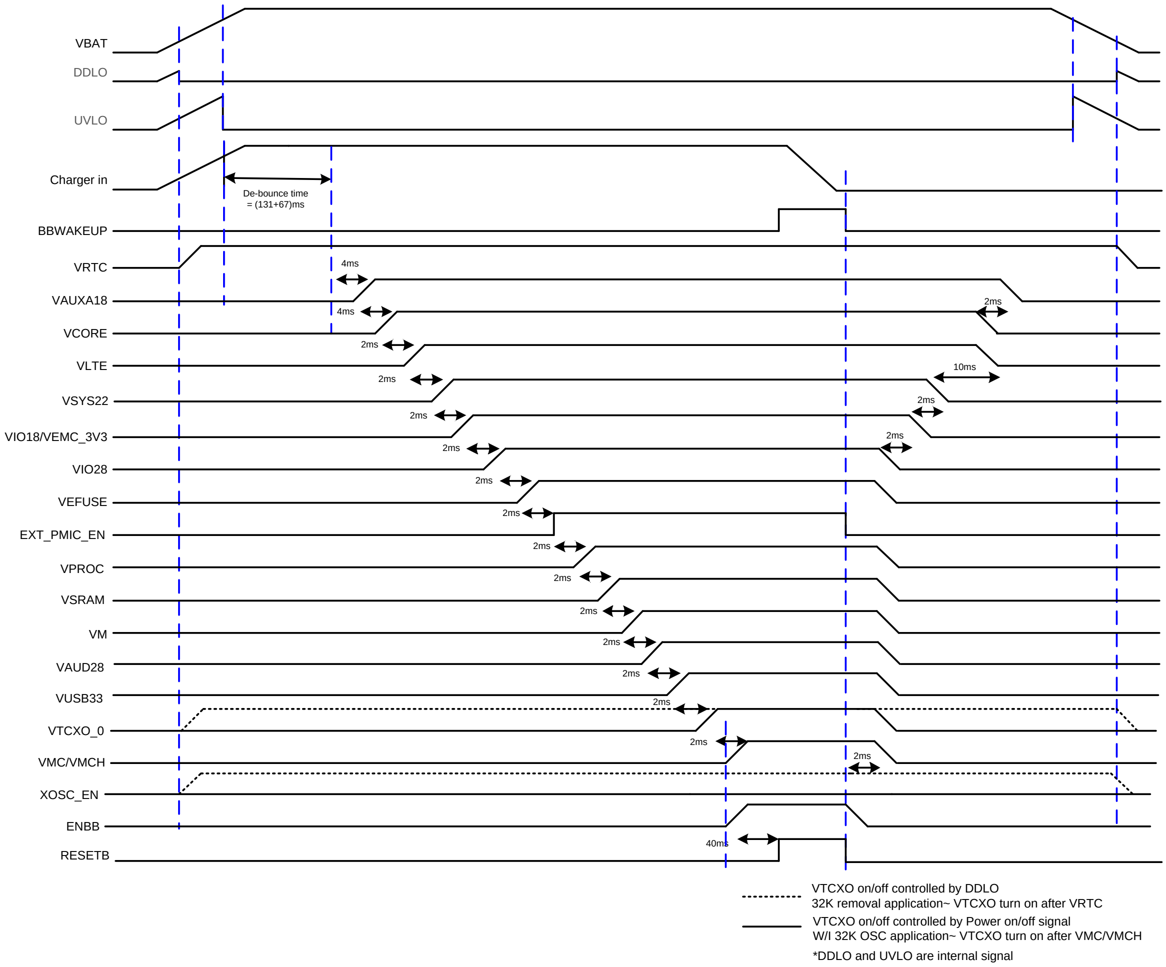

Figure 3-3. Power-on/off control sequence with XTAL by charger plug in

1. Pushing PWRKEY (pulling the PWRKEY pin to low level)
   Pulling PWRKEY low is a typical method to turn on the handset. The system reset ends at the moment when all default-on regulators are sequentially turned on. After that, the baseband will send the BBWAKEUP signal back to PMIC for acknowledgement. To successfully power on the handset, PWRKEY should be kept low until PMIC receives BBWAKEUP from the baseband.

2. RTC module generates BBWAKEUP to wake up the system.
   If the RTC module is scheduled to wake up the handset at some time, the BBWAKEUP signal will be directly sent to PMIC. In this case, BBWAKEUP becomes high at specific moment and allows PMIC power-on. This is called the RTC alarm.

3. Valid charger plug-in (CHRIN voltage within valid range)
   The charger plug-in will also turn on the handset if the charger is valid. When PMU_CHGIN input voltage> CHGIN_VTHH and VSYS>UVLO, the handset will also be powered on.

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Under-voltage lockout (UVLO)

The UVLO state in PMIC prevents start-up if the initial voltage of the main battery is below UVLO_VTH. The judgment is done by VSYSNS (with charger plugged in) and VBATSNS+VSYSNS (without charger plugged in). It ensures that the handset is powered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator which ensures smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO state and PMIC will be turned off by itself, except for VRTC LDO, to prevent further discharging. Once PMIC enters the UVLO state, it will draw low quiescent current. RTC LDO will still be working until DDLO disables it.

Deep discharge lockout (DDLO)

PMIC will enter the deep discharge lockout (DDLO) state when the battery voltage drops below DDLO_VTHL. In this state, VRTC LDO will be shut down. Otherwise, it will draw very low quiescent current to prevent further discharging or even damage to the cells.

Reset

PMIC contains a reset control circuit which takes effect at both power-up and power-down. The RESETB pin is held low in the beginning of power-up and returns to high after the pre-determined delay time. The delay time is controlled by a large counter, which uses the clock from the internal ring-oscillator. At power-off, the RESETB pin will return to low immediately without any delay.

Over-temperature protection

If the die temperature of PMIC exceeds 150°C, PMIC will automatically disable all regulators except for VRTC. Once the over-temperature state is resolved, a new power-on sequence will be required to enable the regulators.

3.2.2 Buck Converter and Application Reference

There are 5 buck converters in MT6328 to efficiently generate regulated power for graphic processor, digital core and circuits. The block diagram is shown in Figure 3-1. The buck converters operate with 3 or 2MHz fixed frequency pulse width modulation (PWM) mode at moderate to heavy load currents. At light load currents, the converter automatically enters Pulse Frequency Modulation (PFM) mode to save power and improve light load efficiency. It also has a force-PWM mode option to allow the converter to remain in the PWM mode regardless of the load current, so that the noise spectrum of the converter can be minimized for certain highly-noise-sensitive handset applications. The buck converters also have an internal Over-Current Protection (OCP) circuit to limit the maximum high-side power FET current in over-load conditions. It has an internal soft start circuit to control the ramp-up rate of the output voltage during start-up.

Table 3-1. Buck converter brief specifications

BUCK name	Default Voltage (V)	Vout (Volt)	Voltage step (mV)	Imax (mA)	Default on (Y/N)	Application

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BUCK name	Default Voltage (V)	Vout (Volt)	Voltage step (mV)	Imax (mA)	Default on (Y/N)	Application
VPROC	1.15	0.6~1.31	6.25	5000	Y	CPU
VCORE1	1.15	0.6~1.31	6.25	3500	Y	Digital core always on domain (CORE_AO)
VLTE	1.05	0.6~1.31	6.25	2800	Y	Digital core power down domain (CORE_PDN)
VSYS22	2.0	2.0/2.2	NA	1900	Y	SYS LDOs power
VPA	0.0	0.5~3.4	50	600	N	3G/LTE PA

3.2.3 Low Dropout Regulator (LDOs) and Application Reference

Table 3-2. LDO types and brief specifications

Type	LDO name	Input power domain	Default Voltage	Vout (Volt)	Imax (mA)	Default on (Y/N)	Application
ALDO	VTCXO_0	AVDD45_LDO2	2.8	2.8	40	Y	26MHz reference clock
ALDO	VTCXO_1	AVDD45_LDO1	2.8	2.8	40	N	26MHz reference clock
ALDO	VAUD28	AVDD45_LDO1	2.8	2.8	40	Y	Audio
ALDO	VAUXA18	AVDD45_LDO1	1.8	1.8	40	Y	AUXADC
ALDO	VCAMA	AVDD45_LDO1	2.8	1.5/1.8/2.5/2.8	200	N	Camera module
ALDO	VCN28	AVDD45_LDO1	2.8	2.8	40	N	Connectivity 2.8V
ALDO	VRF18_0	AVDD22_LDO3	1.825	1.825	350	N	RF power
ALDO	VRF18_1	AVDD22_LDO4	1.825	1.825	300	N	RF power
ALDO	TREF	VBAT_LDOS1	1.8	1.8	1	N	Battery interface
DLDO	VSIM1	AVDD45_LDO4	1.8	1.7/1.8/1.86/2.76/3.0/3.1	50	N	1st SIM card
DLDO	VSIM2	AVDD45_LDO4	1.8	1.7/1.8/1.86/2.76/3.0/3.1	50	N	2nd SIM card

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Type	LDO name	Input power domain	Default Voltage	Vout (Volt)	Imax (mA)	Default on (Y/N)	Application
DLDO	VCAM_AF	AVDD45_LDO5	2.8	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	N	Camera module
DLDO	VGP1	AVDD45_LDO3	2.8	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	N	Cap touch
DLDO	VMC	AVDD45_LDO5	2.9	1.8/2.9/3.0/3.3	200	Y	SD 2.0/3.0 memory card
DLDO	VMCH	AVDD45_LDO2	2.9	2.9/3.0/3.3	800	Y	SD 3.0 memory card
DLDO	VEMC_3V3	AVDD45_LDO4	2.9	2.9/3.0/3.3	400	Y	eMMC 3.3V
DLDO	VIO28	AVDD45_LDO3	2.8	2.8	200	Y	2V8 IO
DLDO	VCN33	AVDD45_LDO1	3.3	3.3/3.4/3.5/3.6	350	N	Connectivity 3.3V
DLDO	VUSB33	AVDD45_LDO4	3.3	3.3	20	Y	USB 3.3V
DLDO	VEFUSE	AVDD45_LDO4	1.8	1.8/1.9/2.0/2.1/2.2	200	Y	Main chip Efuse power
DLDO	VIO18	AVDD22_LDO2	1.8	1.8	600	Y	1.8V IO
DLDO	VM	AVDD22_LDO1	By HW Trapping	1.24/1.39/1.54	1000	Y	DRAM
DLDO	VCAM_IO	AVDD22_LDO2	1.8	1.2/1.3/1.5/1.8	200	N	Camera module
DLDO	VCN18	AVDD22_LDO2	1.8	1.8	150	N	Connectivity 1.8V
DLDO	VCAMD	AVDD22_LDO1	1.3	0.9/1.0/1.1/1.22/1.3/1.5	500	N	Camera module
DLDO	VSRAM	AVDD22_LDO2	1.2	0.6~1.31	400	Y	CPU SRAM
VRTC	VRTC	AVDD45_LDO2	2.8	2.8	2	Y	Real-time clock
DVDD18_DIG	DVDD18_DIG	AVDD45_LDO2	1.8	1.8	20	Y	Internal digital
VIBR	VIBR	AVDD45_L	2.8	1.2/1.3/1.5/1.8/2	100	N	Vibrator

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Type	LDO name	Input power domain	Default Voltage	Vout (Volt)	Imax (mA)	Default on (Y/N)	Application
		DO5		.5/2.8/3.0/3.3			

3.2.4 Drivers

MT6328 supports 2 indicator LED drivers at most. The following figure depicts the major application for indicator LEDs drivers, and how to configure breath mode.

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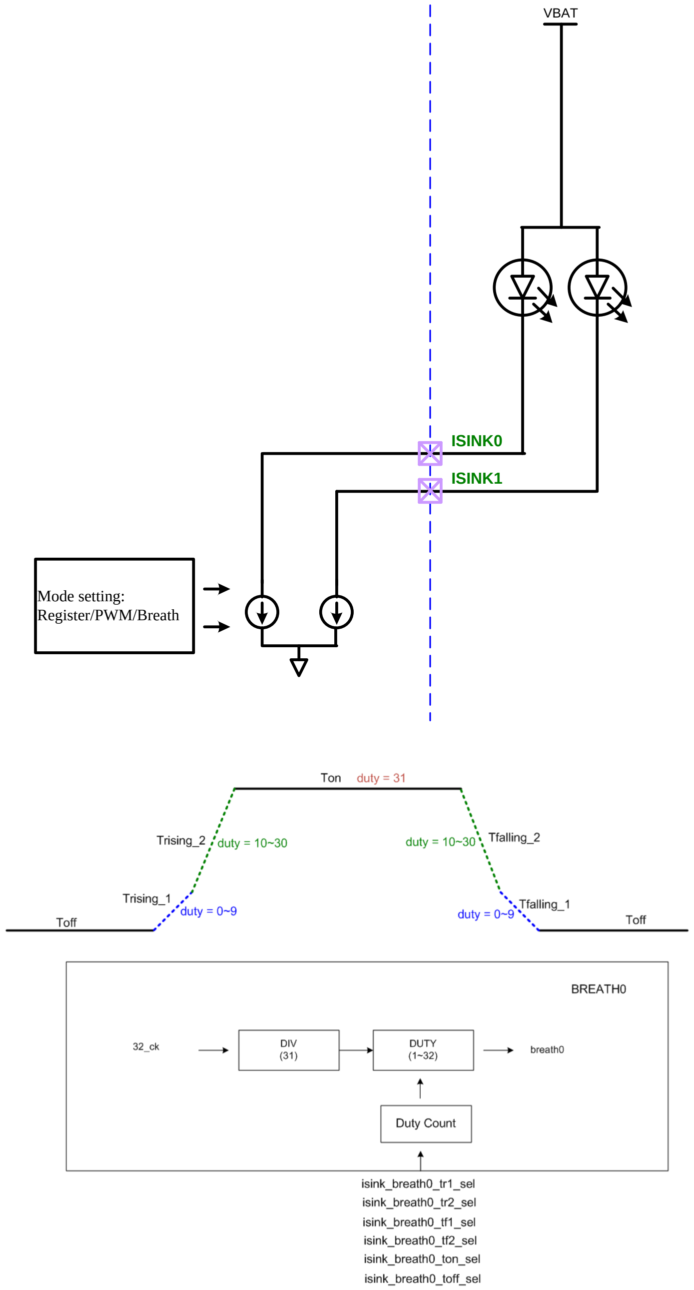

Figure 3-4. Configuration for indicator LED drivers

3.2.5 Vibrator Driver

The VIBR driver power allows up to 100mA current for is for ERM (Eccentric Rotating Mass) or coin type vibrator with programmable output voltage.

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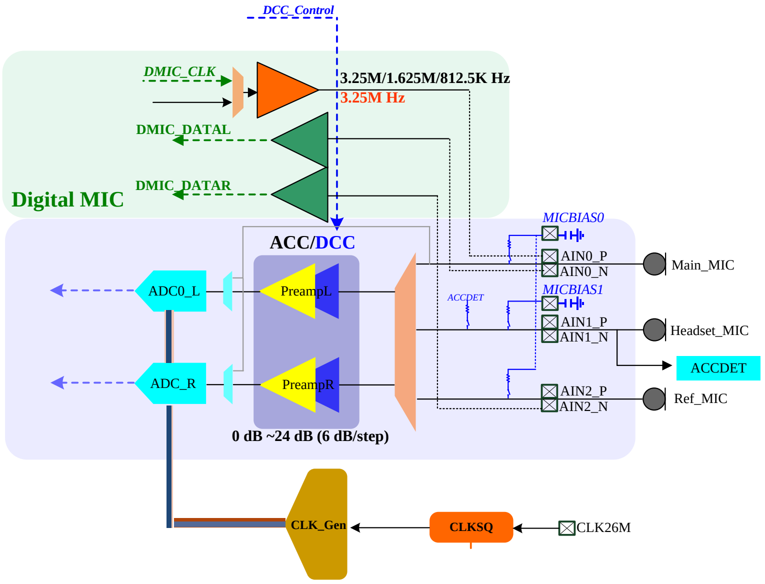
3.2.6 Audio CODEC and Accessory Detection

3.2.6.1 Block Descriptions

The block diagram of audio codec is illustrated below. The audio uplink path is composed of PGA and audio ADC. There are three input pairs of the uplink path to support dual-MIC, earphone-MIC, and digital MIC. The uplink front-end to PGA can be configured as ACC or DCC type. The audio downlink is composed of stereo audio DACs, stereo headphone drivers and a mono voice driver. High-fidelity audio is reproduced on headphones and clear mobile speech on earpiece is driven by voice drivers. The internal high output power loud-speaker amplifier is also embedded. The necessary MIC bias voltages and multi-key accessory detection are also provided by this completed audio codec.



(a) Audio/speech uplink and accessory detection

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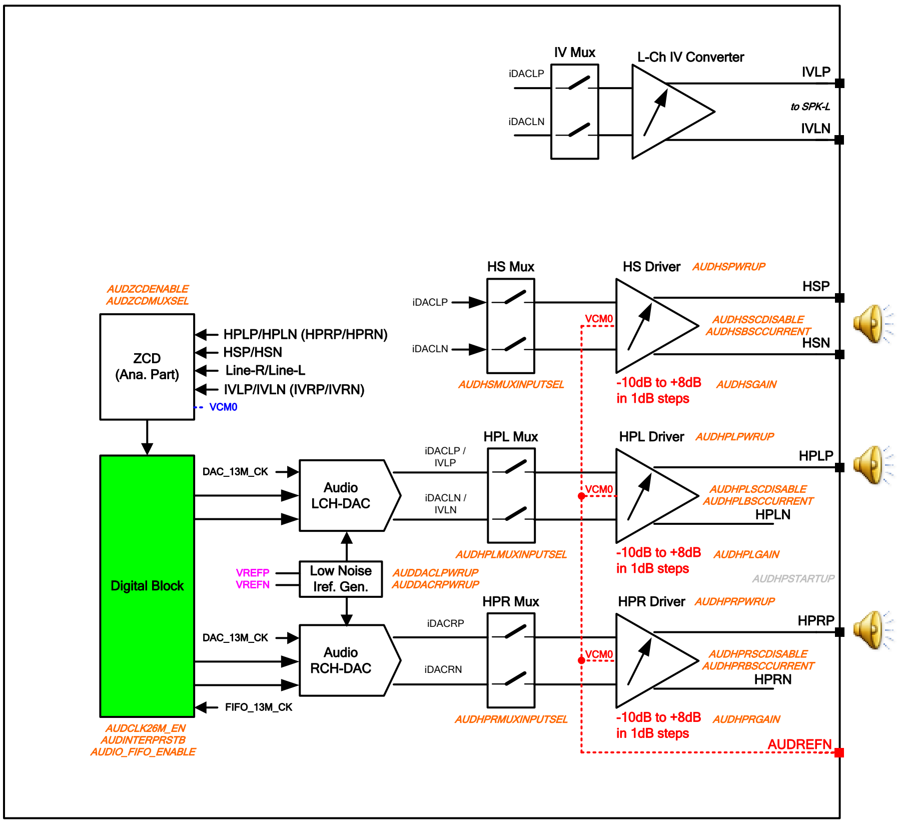

(b) Audio/speech downlink

Figure 3-5. Audio CODEC block diagram

3.2.7 Class-AB/D Audio Amplifier

MT6328 has one built-in channel high efficiency class AB/D audio power amplifier capable of delivering 0.7 watt of power on an 8 ohm BTL load from a 3.7V battery supply. Over-current protection is integrated. MT6328 also has built-in receiver mode for 2-in-1 loudspeaker which supports multi-purpose loudspeaker without any extra BOM cost. The output power can reach 97mW onto 8 ohm speaker load. The block diagram is shown below.

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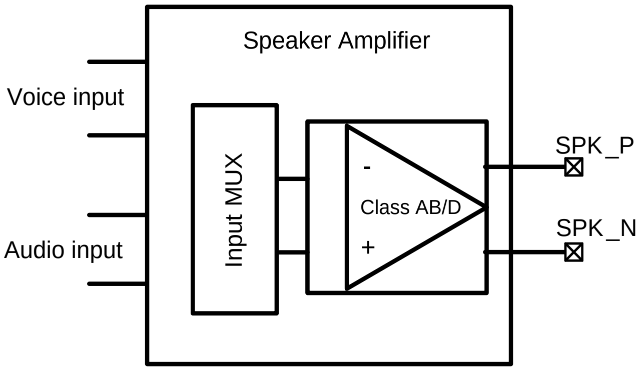

Figure 3-6. Block diagram of class-AB/D

3.2.8 Battery Charger (Charger Controller)

The charger controller senses the charger input voltage from either a standard AC-DC adaptor or an USB charger. When the charger input voltage is within a pre-determined range, the charging process will be activated. This detector resists higher input voltages than other parts of PMIC.

3.2.8.1 Block Descriptions

The block diagram of battery charger is illustrated below.

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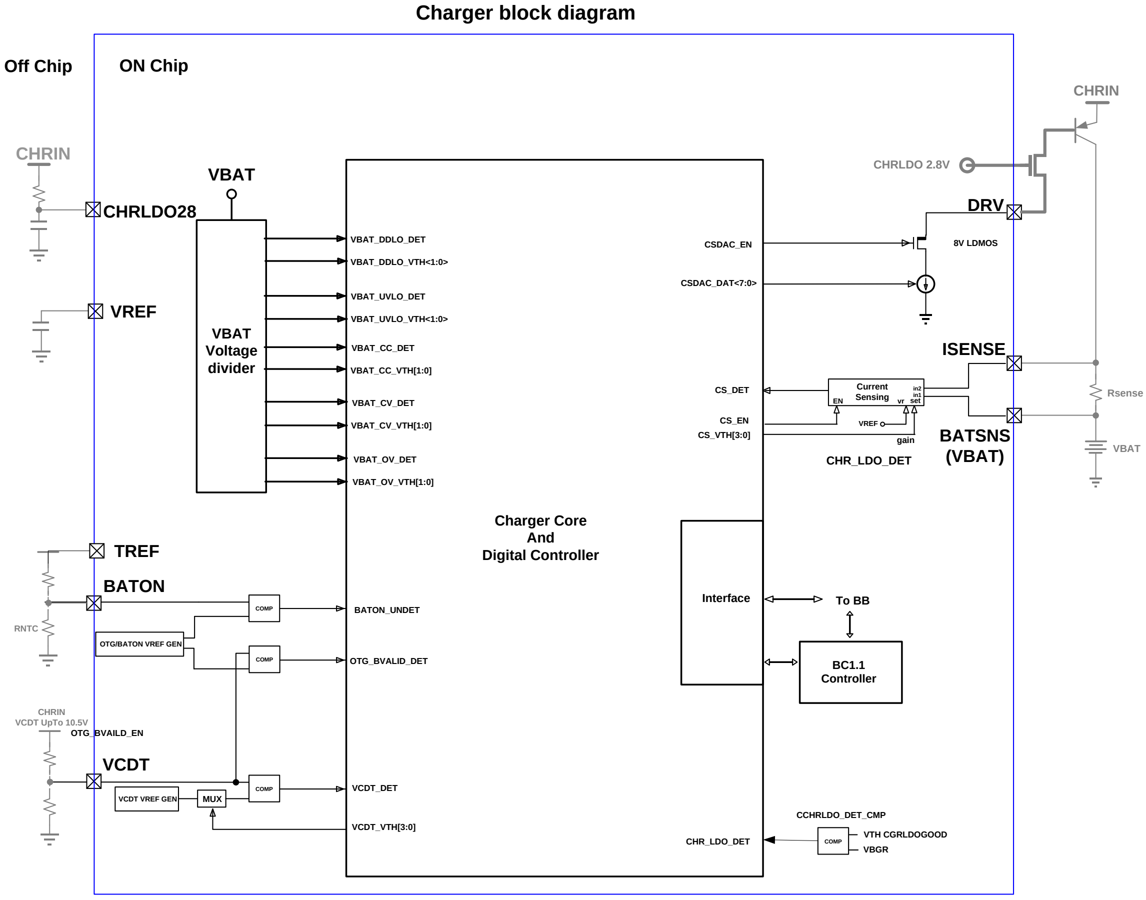

Figure 3-7. Block diagram of battery charger

3.2.8.1.1 Charger Detection

Whenever an invalid charging source is detected (> 7.0V, software default setting), the charger detector will stop the charging process immediately to avoid burning out the chip or even the phone. Furthermore, if the charger-in level is not high enough (< 4.3V), the charger will also be disabled to avoid improper charging behavior.

3.2.8.1.2 Charging Control

When the charger is active, the charger controller will manage the charging phase according to the battery status. During the charging period, the battery voltage is constantly monitored. The battery charger supports pre-charge mode (VBAT < 3.0V, PMIC power-off state), CC mode (Constant Current mode or fast charging mode at the range of 3.0V < VBAT < 4.2V, CV default voltage) and CV mode (Constant Voltage mode) to optimize the charging procedure for Li-ion battery. See the figure below for the charging states diagram.

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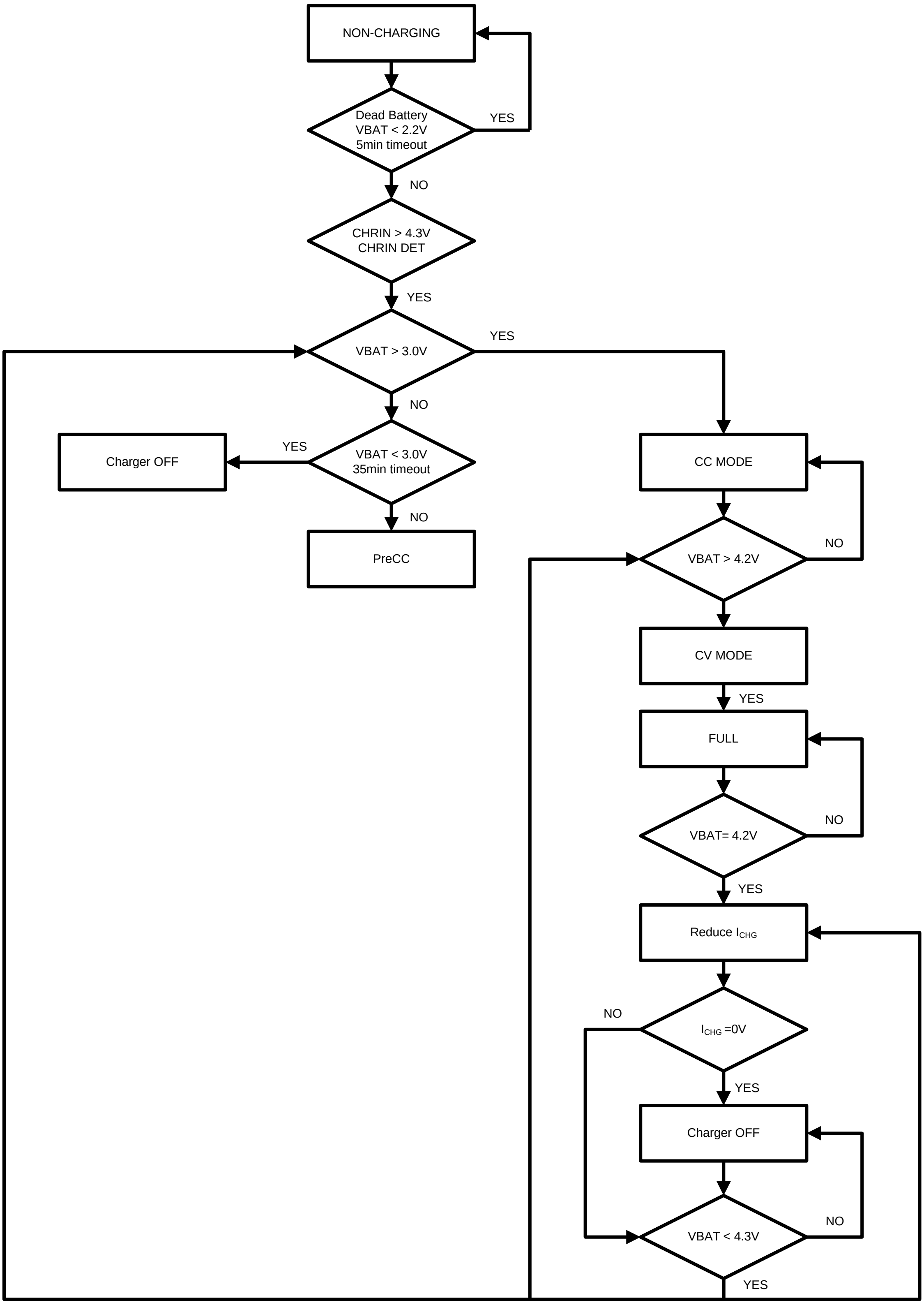

Figure 3-8. Flow chart of charging states

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Pre-charge mode

When the battery voltage is in the UVLO state, the charger will operate in the pre-charge mode. There are two steps in this mode. While the battery voltage is deeply discharged below 2.2V, IUNIT trickle charging current is applied to the battery.

The IUNIT trickle charging current is about 550ms pulse 70mA current when VBAT is under 2.2V.

When the battery voltage exceeds 2.2V, i.e. the PRECC1 stage, the closed-loop pre-charge will be enabled. The voltage drop across the external RSENSE is kept around 16.8mV (AC charger) or 3.92mV (USB host). The closed-loop pre-charge current can be calculated:

$$I_{PRECC1,\ ACadapter} = \frac{V_{SENSE}}{Rsense} = \frac{16.8mV}{Rsense}$$

$$I_{PRECC1,\ USBHOST} = \frac{V_{SENSE}}{Rsense} = \frac{3.92mV}{Rsense}$$

Constant current mode

As the battery is charged up and over 3.0V, it can switch to the CC mode. (CHR_EN should be high) In the CC mode, several charging currents can be set by programming registers or the external RSENSE resistor. The charging current can be determined by CS_VTH/RSENSE, where CS_VTH is programmed by registers. For example, if RSENSE is selected as 0.056ohm, the CC mode charging current can be set from 70 to 2,000mA. It can accommodate the battery charger to various charger inputs with different current capabilities.

Constant-voltage mode and over-voltage protection (OV)

When the battery voltage reaches about 4.2V, a constant voltage is used for charging. This is called the full-voltage charging mode or constant-voltage charging mode in correspondence to a linear charger. When the battery voltage actually reaches 4.2V, the charging current gradually decreased step-by-step, and the end-of-charging process starts. It may prolong the charging and detecting period for acquiring optimized full charging volume. The charging process is completed once the current reaches termination current automatically and this mechanism is optimized for different battery packs. Whenever the battery voltage exceeds 4.3V (programmed by SW), a hardware OV protection will be activated and turns off the charger immediately.

3.2.8.1.3 BC1.x Dead-Battery Support

MT6328 also supports dead-battery condition BC1.x. These specifications protect dead-battery charging by timer and trickle current. Once the battery voltage is below 2.2V, a period (TUNIT) of trickle current (IUNIT) will be applied to the battery.

If the battery voltage is still below 2.2V after the trickle current is applied, the charger will be disabled. On the other hand, once the battery voltage rises to above 2.2V, the charger will enter the PRECC1 stage, and the charging current will be 70mA or 300mA depending on the type of the charging port.

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When the battery is below 3.0V, the charger will charge the battery by the PRECC1 current.
A dedicated 5 min. (T1) timer will be timed out and disable the charger if the battery voltage is always below 2.4V under charging. Another 35 min. (T2) timer will also be timed out and disable the charger if the battery voltage is always kept between 2.7V and 3.0V under charging.

The trickle current (IUNIT) and two dedicated timers protect the charging action if the battery is dead.

3.2.8.1.4 Auto Power-On Mode (USB down load without battery)

MT6328 features a default auto power-on mode (or USB DL without battery) no matter with or without battery. Users can disable auto power-on by adding external pull-high resistor on the FCHR_ENB pin. They can still initiate USB DL (auto power-on) by pressing DL_KEY or under valid BAT_ON information (decided by customers' PCB options). Nonetheless, DL_KEY supports key function in normal mode. The valid BAT_ON information can be detected through battery's NTC when it is connected to pin BAT_ON of MT6328.

3.2.9 AUXADC

3.2.9.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the input channels. Real-world messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 15-bit A/D converter: Converts the multiplexed input signal to 15-bit digital data.

Table 3-3. Application and input range of ADC channels

Channel	Application	Input range [V]
0	BATSNS	2.5 ~ 4.5
1	ISENSE	2.5 ~ 4.5
2	VCDT	0 ~ 1.5
3	BATON	0.1 ~ 1.7
5	ACCDET	0 ~ 1.8
7	AUXADC_VIN	0 ~ 1.8
others	Internal use	N/A

3.2.10 Fuel Gauge

The fuel gauging system includes a dedicated ADC for Li-Ion battery current measurement and utilizes the measurement ADC (AUXADC) for battery voltage and temperature measurement. The battery state-of-charge (SOC) estimation is performed by the software using the three measuring methods and the accumulated current measurement. The application diagram of the fuel gauging system is shown in the figure below, where an external resistor is used to convert the current drawn

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from the battery into a voltage which is then measured by FG ADC. The value of the external resistor must be chosen so that the maximum current during charging or discharging will not cause ADC to exceed its input voltage range.

The principle of operation of the fuel gauge relies on a combination of Coulomb counting and light load battery voltage measurement. Coulomb counting provides an estimate of the charge that has been withdrawn or delivered to the battery, while battery voltage measurement proves a good estimate of the battery SOC under low-load conditions. The battery voltage measurement compensates for error accumulation during the current integration inherent in Coulomb counting. The hardware also includes necessary modes to allow for simultaneous current and voltage measurement which can be utilized to estimate the battery impedance.

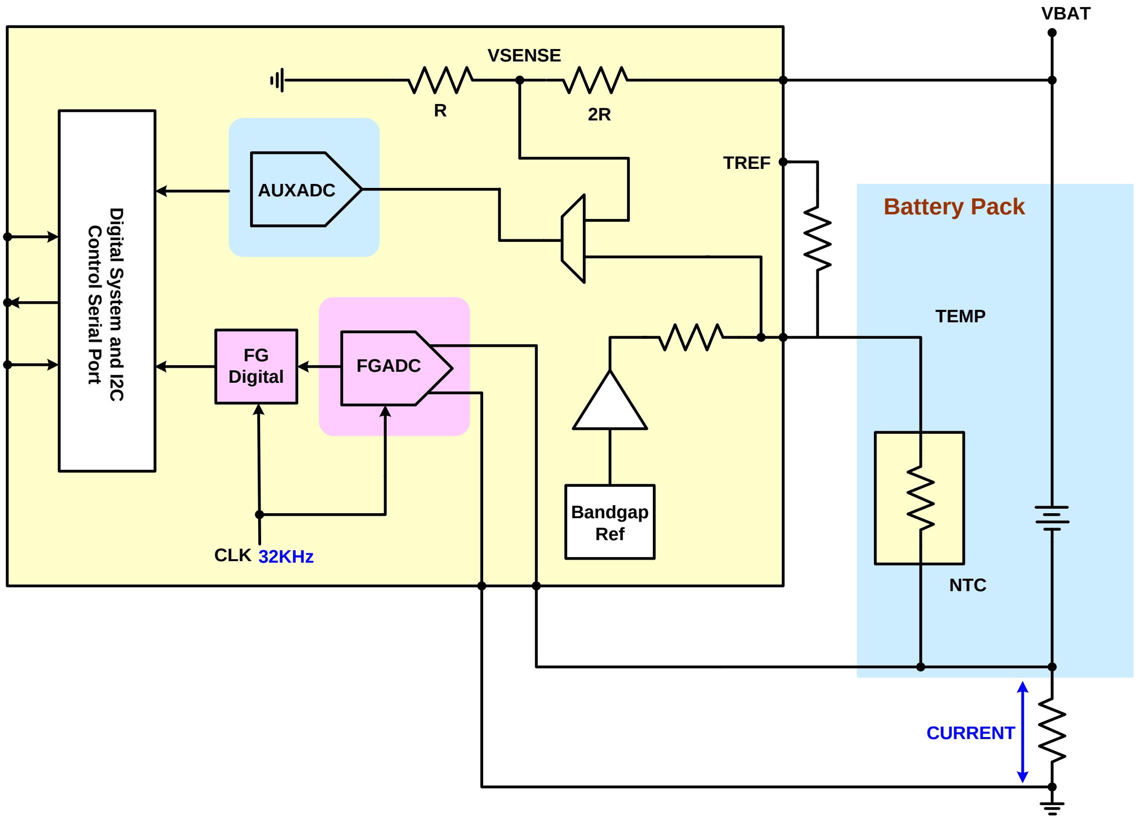

Figure 3-9. Fuel gauge block diagram and external connection

3.2.11 Real-time Clock

The Real Time Clock (RTC) module provides time and data information. The clock is based on a 32.768kHz oscillator with an independent power supply. When the mobile handset is powered off, a dedicated regulator supplies the RTC block. If the main battery is not present, a backup supply such as a small mercury cell battery or a large capacitor will be used. In addition to providing timing data, an alarm interrupt is generated and can be used to power up the baseband core via the BBWAKEUP pin.

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Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches a maximum value (e.g. 59 for seconds and minutes, 23 for hours, etc.). The year span is supported up to 2,127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

In MT6328, RTC module also supports function without 32kHz crystal. It can be configured by hardware option. The two configurations are shown below. While crystal is absent, RTC module has an embedded 32kHz oscillator to assist life time extension after master 32kHz clock is off.

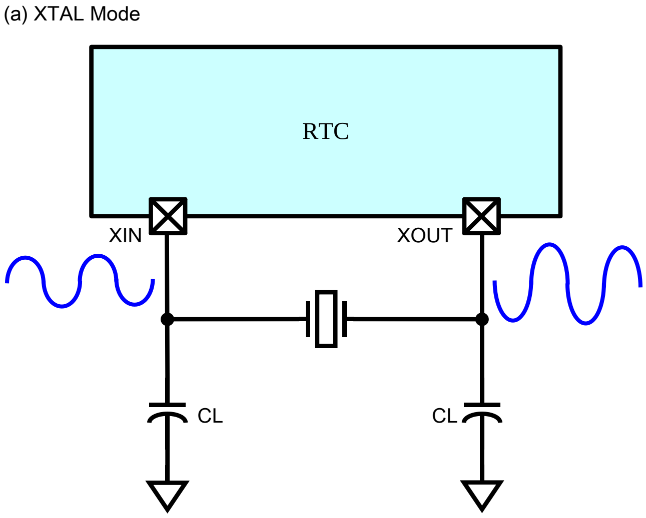

Figure 3-10. RTC configuration methods for XTAL

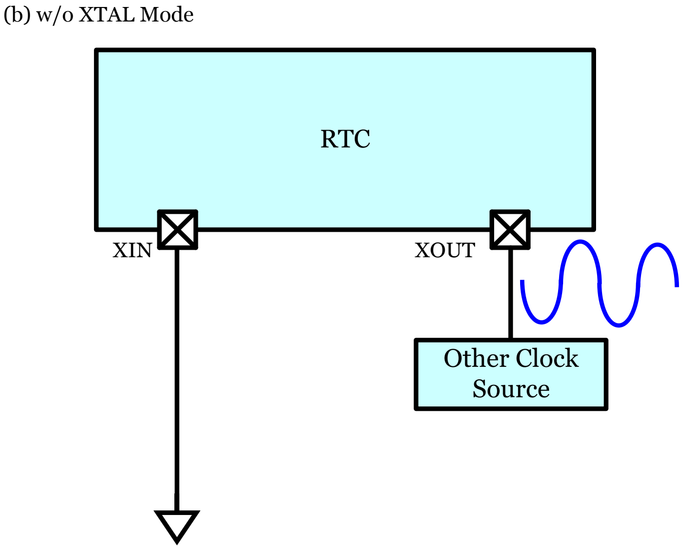

Figure 3-11. RTC configuration methods for w/o XTAL mode

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3.2.11.1 32kHz Crystal Oscillator (XOSC32)

The low-power 32kHz crystal oscillator XOSC32 is designed to work with an external piezoelectric 32.768kHz crystal and a load composed of two functional capacitors. The key performance is shown in the table below.

Table 3-4. Functional specifications of XOSC32

Symbol	Parameter	Min.	Typical	Max.	Unit
VRTC	RTC module power	1.1	2.8	3.0	V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle	20		80	%
I	Current consumption		5		µA
T	Operating temperature	-20		80	°C

The minimum VRTC value means if the crystal oscillator starts up successfully, then the minimum VRTC for the clock to still be alive is 1.1V.

Since the crystal parameters determine the oscillation allowance, below are a few recommendations for the crystal parameters to be used well with XOSC32 in MT6328.

Table 3-5. Recommended parameters of 32kHz crystal

Symbol	Parameter	Min.	Typical	Max.	Unit
F	Frequency range		32768		Hz
GL	Drive level	0.5			uW
Δf/f	Frequency tolerance		+/- 20		ppm
ESR	Series resistance		50	70	KΩ
Co	Static capacitance		0.9	2	pF
CL[1]	Load capacitance	6		12.5	pF

Under such CL range and crystal, the –R is greater than 3 times. If CL is selected larger, the frequency accuracy will be decreased, and the –R will degrade too.

3.2.12 Interrupt and Watchdog

3.2.12.1 Interrupt

Here are interrupt lists of PMIC to inform BB IC:

1. Key pressed and released interrupt
   - PWRKEY: Interrupt is issued when PWRKEY is pressed (and released, set by the register). After receiving the interrupt, the software will read the PWRKEY_DEB status to see if it is pressed or released.

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- HOMEKEY: Interrupt is issued when HOMEKEY is pressed (and released, set by the register). After receiving the interrupt, the software will read the HOMEKEY_DEB status to see if it is pressed or released.

2. Thermal interrupt
   PMIC issues THR_H interrupt for the software high power latch if PMIC die temperature is over thermal regulation high threshold (e.g. 125°c) and issues THR_L for software latch release if PMIC die temperature goes from thermal regulation high threshold (e.g. 125°c) back to under thermal regulation low threshold (e.g. 110°c). The thermal regulation high/low threshold is adjustable.
3. Charger related interrupt
4. Battery voltage/current H/L interrupt
   There are two groups of VBAT detection interrupts.
   1) VBAT detected by AUXADC
      If VBAT is higher than the threshold specified by a register setting, the HIGHBATTERY interrupt will be issued. If VBAT is lower than the threshold specified by another register setting, the LOWBATTERY interrupt will be issued.
   2) VBAT detected by fuel gauge
      If VBAT is higher than the threshold specified by a register setting, the VBAT_H interrupt will be issued. If VBAT is lower than the threshold specified by another register setting, the VBAT_L interrupt will be issued.
5. Fuel-Gauge
6. Speaker OC interrupt
   PMIC supports speaker OC interrupt generation which uses PWM detection method.
7. Buck OC interrupt
   There are 9 bucks and each has its individual interrupt which uses PWM detection method.
8. LDO OC interrupt
   PMIC supports LDO OC interrupt generation. It will be issued if any one of the LDOs has OC condition.
9. RTC interrupt
10. AUDIO interrupt
    Audio interrupt can inform AP playback of the audio status.
11. ACCDET interrupt
    This is for headphone detection.

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Table 3-6. MT6328 interrupts

Module name	Interrupt Name	ENABLE	ENABLE ADR	STATUS	STATUS ADR	Level/Edge	Default EN	De-bounce time	Status Clear Condition
STRUP	PWRKEY	RG_INT_EN_PWRKEY	0x029C bit0	RG_INT_STATUS_PWRKEY	0x02B4 bit0	edge(rising & falling)	1	50ms (in STRUP)	Write 1 Clear
STRUP	HOMEKEY	RG_INT_EN_HOMEKEY	0x029C bit1	RG_INT_STATUS_HOMEKEY	0x02B4 bit1	edge(rising & falling)	0	50ms (in STRUP)	Write 1 Clear
STRUP	PWRKEY_R	RG_INT_EN_PWRKEY_R	0x029C bit2	RG_INT_STATUS_PWRKEY_R	0x02B4 bit2	edge(rising)	1	50ms (in STRUP)	Write 1 Clear
STRUP	HOMEKEY_R	RG_INT_EN_HOMEKEY_R	0x029C bit3	RG_INT_STATUS_HOMEKEY_R	0x02B4 bit3	edge(rising)	0	50ms (in STRUP)	Write 1 Clear
AUXADC	THR_H	RG_INT_EN_THR_H	0x029C bit4	RG_INT_STATUS_THR_H	0x02B4 bit4	edge(rising)	0	50ms (in STRUP)	Write 1 Clear
AUXADC	THR_L	RG_INT_EN_THR_L	0x029C bit5	RG_INT_STATUS_THR_L	0x02B4 bit5	edge(rising)	0	50ms (in STRUP)	Write 1 Clear
AUXADC	BAT_H	RG_INT_EN_BAT_H	0x029C bit6	RG_INT_STATUS_BAT_H	0x02B4 bit6	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	BAT_L	RG_INT_EN_BAT_L	0x029C bit7	RG_INT_STATUS_BAT_L	0x02B4 bit7	level (high active)	0	V (in AUXADC)	Write 1 Clear
RTC	RTC	RG_INT_EN_RTC	0x029C bit9	RG_INT_STATUS_RTC	0x02B4 bit9	level (low active)	0	No	Write 1 Clear
Audio	AUDIO	RG_INT_EN_AUDIO	0x029C bit10	RG_INT_STATUS_AUDIO	0x02B4 bit10	level (high active)	0	No	Write 1 Clear
Accdet	ACCDET	RG_INT_EN_ACCDET	0x029C bit12	RG_INT_STATUS_ACCDET	0x02B4 bit12	level (high active)	0	No	Write 1 Clear
Accdet	ACCDET_EINT	RG_INT_EN_ACCDET_EINT	0x029C bit13	RG_INT_STATUS_ACCDET_EINT	0x02B4 bit13	level (high active)	0	No	Write 1 Clear
Accdet	ACCDET_NEGV	RG_INT_EN_ACCDET_NEGV	0x029C bit14	RG_INT_STATUS_ACCDET_NEGV	0x02B4 bit14	level (high active)	0	No	Write 1 Clear
STRUP	NI_LBAT_INT	RG_INT_EN_NI_LBAT_INT	0x029C bit15	RG_INT_STATUS_NI_LBAT_INT	0x02B4 bit15	edge(rising)	0	150us (in STRUP)	Write 1 Clear
Regulator	VPROC_OC	RG_INT_EN_VPROC_OC	0x02A2 bit0	RG_INT_STATUS_VPROC_OC	0x02B6 bit0	level (high active)	0	PMW deb (in	Write 1

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Module name	Interrupt Name	ENABLE	ENABLE ADR	STATUS	STATUS ADR	Level/Edge	Default EN	De-bounce time	Status Clear Condition
								STRUP)	Clear
Regulator	VSYS_OC	RG_INT_EN_VSYS_OC	0x02A2 bit1	RG_INT_STATUS_VSYS_OC	0x02B6 bit1	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
Regulator	VLTE_OC	RG_INT_EN_VLTE_OC	0x02A2bit2	RG_INT_STATUS_VLTE_OC	0x02B6 bit2	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
Regulator	VCORE_OC	RG_INT_EN_VCORE_OC	0x02A2 bit5	RG_INT_STATUS_VCORE_OC	0x02B6 bit5	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
Regulator	VPA_OC	RG_INT_EN_VPA_OC	0x02A2 bit8	RG_INT_STATUS_VPA_OC	0x02B6 bit8	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
LDO	LDO_OC	RG_INT_EN_LDO_OC	0x02A2 bit9	RG_INT_STATUS_LDO_OC	0x02B6 bit9	level (high active)	1	100/200/400/800us (in INTCTRL)	Write 1 Clear
AUXADC	BAT2_H	RG_INT_EN_BAT2_H	0x02A2 bit10	RG_INT_STATUS_BAT2_H	0x02B6 bit10	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	BAT2_L	RG_INT_EN_BAT2_L	0x02A2 bit11	RG_INT_STATUS_BAT2_L	0x02B6 bit11	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	VISMPS0_H	RG_INT_EN_VISMPS0_H	0x02A2 bit12	RG_INT_STATUS_VISMPS0_H	0x02B6 bit12	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	VISMPS0_L	RG_INT_EN_VISMPS0_L	0x02A2 bit13	RG_INT_STATUS_VISMPS0_L	0x02B6 bit13	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	AUXADC_IMP	RG_INT_EN_AUXADC_IMP	0x02A2 bit14	RG_INT_STATUS_AUXADC_IMP	0x02B6 bit14	level (high active)	0	V (in AUXADC)	Write 1 Clear
Speaker	SPKL_D	RG_INT_EN_SPKL_D	0x02A8 bit0	RG_INT_STATUS_SPKL_D	0X02B8 bit0	level (high active)	0	V (in SPK)	Write 1 Clear
Speaker	SPKL_AB	RG_INT_EN_SPKL_AB	0x02A8 bit1	RG_INT_STATUS_SPKL_AB	0X02B8 bit1	level (high active)	0	V (in SPK)	Write 1 Clear
Charger	OV	RG_INT_EN_OV	0x02A8 bit2	RG_INT_STATUS_OV	0X02B8 bit2	edge(rising)	1	4us (in PCHR_DIG)	Write 1 Clear
Charger	BVALID_DET	RG_INT_EN_BVALID_DET	0x02A8 bit3	RG_INT_STATUS_BVALID_DET	0X02B8 bit3	level (high active)	1	0/100/200/400us (in INTCTRL)	Write 1 Clear
Charger	RGS_BATON_HV	RG_INT_EN_RGS_BATON_HV	0x02A8 bit4	RG_INT_STATUS_RGS_BATON_HV	0X02B8 bit4	level (high active)	1	N	Write 1 Clear

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Module name	Interrupt Name	ENABLE	ENABLE ADR	STATUS	STATUS ADR	Level/Edge	Default EN	De-bounce time	Status Clear Condition
Charger	VBATON_UNDET	RG_INT_EN_VBATON_UNDET	0x02A8 bit5	RG_INT_STATUS_VBATON_UNDET	0X02B8 bit5	level (high active)	1	0/100/200/400us (in INTCTRL)	Write 1 Clear
Charger	WATCHDOG	RG_INT_EN_WATCHDOG	0x02A8 bit6	RG_INT_STATUS_WATCHDOG	0X02B8 bit6	level (high active)	1	N	Write 1 Clear

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3.2.12.2 Watchdog Reset

WDTRSTB_IN is the watchdog reset from AP. PMIC resets all modules to initial state when receiving watchdog reset from AP.

3.2.13 SPI Interface

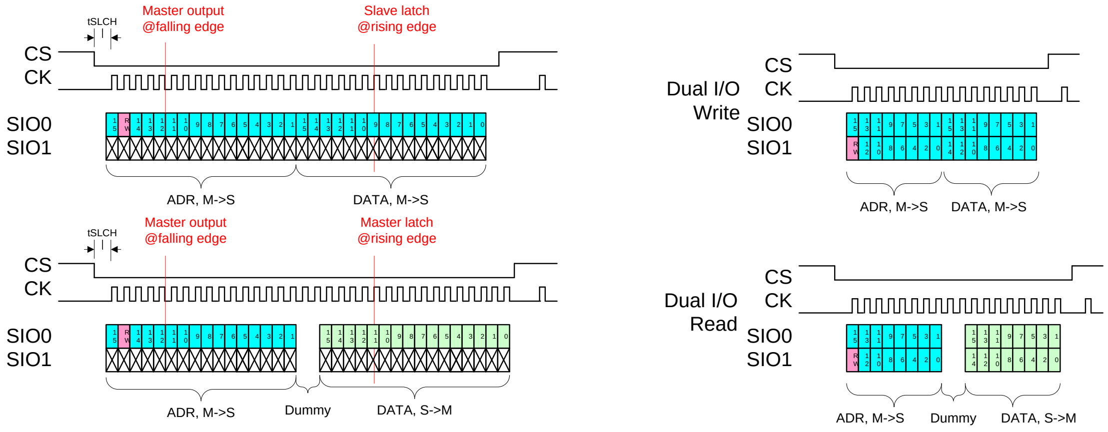
PMIC uses a 4-wire interface consisting of a clock, a chip select and two data signals (MOSI and MISO) to connect to BB. This serial-parallel interface allows BB to write commands to and read status from PMIC.

On the other hand, the IO pin (MISO) can be used as data pin or interrupt pin depending on what the system scenario is. It is used as data pin when system is in normal mode but as INT pin when system is in suspend mode.

3.2.13.1 Data Format

The pre-defined SPI format consists of two modes: Single I/O mode and dual I/O mode. Single I/O always uses MOSI as output and input. Dual I/O uses both MOSI and MISO to be output and input to achieve better channel usage. The format conveys information of R/W direction, 15-bit address (bit 15 to bit 1) and 16-bit data, and both addresses and data are MSB first. The operation waveform of SPI is illustrated as below. The SPI slave in PMIC latch data sent from the master at rising edge of clock, and output data at falling edge of clock. The parameter tSLCH, tDMMY and tCHSH are fully configurable through command registers (in BB instead of PMIC) as illustrated in the figures below.

SPI format:



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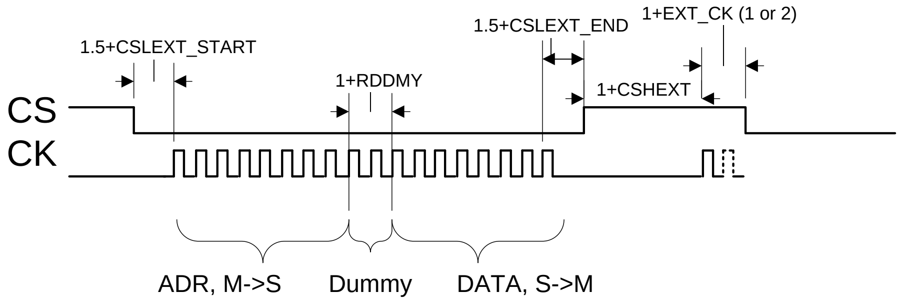
SPI parameter configuration:



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3.2.14 GPIO

3.2.14.1 GPIO List

Table 3-7. MT6328 GPIO list

Pin Name	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.5	Aux Func.6	Aux Func.7	PU/PD
PAD_HOMEKEY	GPIO0	**I1:HOMEKEY**	O:INT_0	I0:TEST_CK0			**PU**/PD
PAD_SRCLKEN_IN0	GPIO1	**I1:SRCLKEN_IN0**			I0:TEST_IN0	O:TEST_OUT0	**PU**/PD
PAD_SRCLKEN_IN1	GPIO2	**I1:SRCLKEN_IN1**			I0:TEST_IN1	O:TEST_OUT1	**PU**/PD
PAD_RTC32K_1V8_0	GPIO3	**O:RTC_32K1V8_0**			I0:TEST_IN2	O:TEST_OUT2	PU/PD
PAD_RTC32K_1V8_1	GPIO4	**O:RTC_32K1V8_1**	O:INT_1	I0:TEST_CK2	I0:TEST_IN3	O:TEST_OUT3	PU/PD
PAD_SPI_CLK	GPIO5	**I0:SPI_CLK**					PU/**PD**
PAD_SPI_CSN	GPIO6	**I1:SPI_CSN**					**PU**/PD
PAD_SPI_MOSI	GPIO7	**B0:SPI_MOSI**					PU/**PD**
PAD_SPI_MISO	GPIO8	**B0:SPI_MISO**					PU/**PD**
PAD_AUD_CLK	GPIO9	**I0:AUD_CLK**		I0:TEST_CK1			PU/**PD**
PAD_AUD_DAT_MOSI	GPIO10	**I0:AUD_DAT_MOSI**			I0:TEST_IN4	O:TEST_OUT4	PU/**PD**
PAD_AUD_DAT_MISO	GPIO11	**O:AUD_DAT_MISO**			I0:TEST_IN5	O:TEST_OUT5	PU/**PD**
PAD_ENBB	GPIO12	**O:ENBB**			I0:TEST_IN6	O:TEST_OUT6	PU/**PD**
PAD_XOSC_EN	GPIO13	**O:XOSC_EN**					PU/**PD**

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3.2.14.2 GPIO Specification

Table 3-8. MT6328 GPIO electrical characteristics

Parameters	Descriptions	Min.	Typ.	Max.	Unit
Inputs					
VIH	Input logic low voltage	0.65*VDDQ		VDDQ+0.3	V
VIL	Input logic high voltage	-0.3		0.35*VDDQ	V
Rpu	Input pull-up resistance	40	75	190	KΩ
Rpd	Input pull-down resistance	40	75	190	KΩ
Outputs					
VOH (DC)	DC Output logic low voltage	0.75*VDDQ			V
VOL (DC)	DC Output logic high voltage			0.25*VDDQ	V
Leakage					
IIN	Input leakage current (any input 0V<VIN<VDDIO)	-5		5	mA
IOZ	Tri-state output leakage current	-5		5	mA
IIN	Input leakage current (VIN=3.3V/0V) for floating nwell IO	-10		10	mA
IOZ	Tri-state output leakage current for floating nwell IO	-10		10	mA

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3.3 Register Table and Descriptions

Module name: PMIC_REG Base address: (+0h)

Address	Name	Width	Register Function
0000	STRUP_CON0	16	STRUP Control Register 0
0002	STRUP_CON2	16	STRUP Control Register 2
0004	STRUP_CON3	16	STRUP Control Register 3
0008	STRUP_CON5	16	STRUP Control Register 5
0010	STRUP_CON9	16	STRUP Control Register 9
0012	STRUP_CON10	16	STRUP control register 10
0014	STRUP_CON11	16	STRUP Control Register 11
0018	STRUP_CON13	16	STRUP Control Register 13
001A	STRUP_CON14	16	STRUP Control Register 14
001C	STRUP_CON15	16	STRUP Control Register 15
001E	STRUP_CON16	16	STRUP Control Register 16
0040	STRUP_ANA_CON0	16	STRUP ANA Control Register 0
0206	TEST_OUT	16	TEST_OUT
0220	TOPSTATUS	16	TOP Status
0222	TDSEL_CON	16	TDSEL_CON
0224	RDSEL_CON	16	RDSEL_CON
0226	SMT_CON0	16	SMT_CON0
0228	SMT_CON1	16	SMT_CON1
022A	SMT_CON2	16	SMT_CON2
022C	DRV_CON0	16	DRV_CON0
022E	DRV_CON1	16	DRV_CON1
0230	DRV_CON2	16	DRV_CON2
0232	DRV_CON3	16	DRV_CON3
0234	TOP_STATUS	16	TOP_STATUS
023A	RGS_ANA_MON	16	RGS_ANA_MON
023C	TOP_CKPDN_CON0	16	TOP_CKPDN Control Register 0
023E	TOP_CKPDN_CON0_SET	16	TOP_CKPDN_CON0 Register SET
0240	TOP_CKPDN_CON0_CLR	16	TOP_CKPDN_CON0 Register CLR
0242	TOP_CKPDN_CON1	16	TOP_CKPDN Control Register 1
0244	TOP_CKPDN_CON1_SET	16	TOP_CKPDN_CON1 Register SET
0246	TOP_CKPDN_CON1_CLR	16	TOP_CKPDN_CON1 Register CLR
0248	TOP_CKPDN_CON2	16	TOP_CKPDN Control Register 2
024A	TOP_CKPDN_CON2_SET	16	TOP_CKPDN_CON2 Register SET
024C	TOP_CKPDN_CON2_CLR	16	TOP_CKPDN_CON2 Register CLR

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Address	Name	Width	Register Function
024E	TOP_CKPDN_CON3	16	TOP_CKPDN control register 3
0250	TOP_CKPDN_CON3_SET	16	TOP_CKPDN_CON3 Register SET
0252	TOP_CKPDN_CON3_CLR	16	TOP_CKPDN_CON3 Register CLR
0254	TOP_CKPDN_CON4	16	TOP_CKPDN control register 4
0256	TOP_CKPDN_CON4_SET	16	TOP_CKPDN_CON4 Register SET
0258	TOP_CKPDN_CON4_CLR	16	TOP_CKPDN_CON4 Register CLR
025A	TOP_CKSEL_CON0	16	TOP_CKSEL Control Register 0
025C	TOP_CKSEL_CON0_SET	16	TOP_CKSEL_CON0 Register SET
025E	TOP_CKSEL_CON0_CLR	16	TOP_CKSEL_CON0 Register CLR
0260	TOP_CKSEL_CON1	16	TOP_CKSEL control register 1
0262	TOP_CKSEL_CON1_SET	16	TOP_CKSEL_CON1 Register SET
0264	TOP_CKSEL_CON1_CLR	16	TOP_CKSEL_CON1 Register CLR
0266	TOP_CKSEL_CON2	16	TOP_CKSEL Control Register 2
0268	TOP_CKSEL_CON2_SET	16	TOP_CKSEL_CON2 Register SET
026A	TOP_CKSEL_CON2_CLR	16	TOP_CKSEL_CON2 Register CLR
026C	TOP_CKDIVSEL_CON0	16	TOP_CKDIVSEL Control Register 0
026E	TOP_CKDIVSEL_CON0_SET	16	TOP_CKDIVSEL_CON0 Register SET
0270	TOP_CKDIVSEL_CON0_CLR	16	TOP_CKDIVSEL_CON0 Register CLR
0272	TOP_CKDIVSEL_CON1	16	TOP_CKDIVSEL Control Register 1
0274	TOP_CKDIVSEL_CON1_SET	16	TOP_CKDIVSEL_CON1 Register SET
0276	TOP_CKDIVSEL_CON1_CLR	16	TOP_CKDIVSEL_CON1 Register CLR
0278	TOP_CKHWEN_CON0	16	TOP_CKHWEN control register 0
027A	TOP_CKHWEN_CON0_SET	16	TOP_CKHWEN_CON0 Register SET
027C	TOP_CKHWEN_CON0_CLR	16	TOP_CKHWEN_CON0 Register CLR
027E	TOP_CKHWEN_CON1	16	TOP_CKHWEN control register 1
0280	TOP_CKHWEN_CON1_SET	16	TOP_CKHWEN_CON1 Register SET
0282	TOP_CKHWEN_CON1_CLR	16	TOP_CKHWEN_CON1 Register CLR

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Address	Name	Width	Register Function
028A	**TOP_CLKSQ**	16	TOP_CLKSQ Register
028C	**TOP_CLKSQ_SET**	16	TOP_CLKSQ Register SET
028E	**TOP_CLKSQ_CLR**	16	TOP_CLKSQ Register CLR
0290	**TOP_CLKSQ_RTC**	16	TOP_CLKSQ_RTC Register
0292	**TOP_CLKSQ_RTC_SET**	16	TOP_CLKSQ_RTC Register SET
0294	**TOP_CLKSQ_RTC_CLR**	16	TOP_CLKSQ_RTC Register CLR
0296	**TOP_CLK_TRIM**	16	TOP_CLK_TRIM Register
0418	**BUCK_ALL_CON18**	16	Buck All Control Register 18
041A	**BUCK_ALL_CON19**	16	Buck All Control Register 19
0420	**BUCK_ALL_CON22**	16	Buck All Control Register 22
042E	**SMPS_TOP_ANA_CON0**	16	SMPS_TOP Control Register 0
0430	**SMPS_TOP_ANA_CON1**	16	SMPS_TOP control register 1
0432	**SMPS_TOP_ANA_CON2**	16	SMPS_TOP control register 2
0434	**SMPS_TOP_ANA_CON3**	16	SMPS_TOP control register 3
0436	**SMPS_TOP_ANA_CON4**	16	SMPS_TOP control register 4
0438	**SMPS_TOP_ANA_CON5**	16	SMPS_TOP control register 5
043A	**SMPS_TOP_ANA_CON6**	16	SMPS_TOP Control Register 6
043C	**SMPS_TOP_ANA_CON7**	16	SMPS_TOP Control Register 7
0440	**VCORE_ANA_CON0**	16	VCORE_ANA Control Register 0
0442	**VCORE_ANA_CON1**	16	VCORE_ANA Control Register 1
0444	**VCORE_ANA_CON2**	16	VCORE_ANA Control Register 2
0446	**VCORE_ANA_CON3**	16	VCORE_ANA Control Register 3
0448	**VCORE_ANA_CON4**	16	VCORE_ANA Control Register 4
044A	**VSYS22_ANA_CON0**	16	VSYS22_ANA Control Register 0
044C	**VSYS22_ANA_CON1**	16	VSYS22_ANA Control Register 1
044E	**VSYS22_ANA_CON2**	16	VSYS22_ANA Control Register 2
0450	**VSYS22_ANA_CON3**	16	VSYS22_ANA Control Register 3
0452	**VSYS22_ANA_**	16	VSYS22_ANA Control Register 4

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Address	Name	Width	Register Function
	CON4		
0454	VPROC_ANA_CON0	16	VPROC_ANA Control Register 0
0456	VPROC_ANA_CON1	16	VPROC_ANA Control Register 1
0458	VPROC_ANA_CON2	16	VPROC_ANA Control Register 2
045A	VPROC_ANA_CON3	16	VPROC_ANA Control Register 3
045C	VPROC_ANA_CON4	16	VPROC_ANA Control Register 4
045E	OSC32_ANA_CON0	16	OSC32 Control Register 0
0460	OSC32_ANA_CON1	16	OSC32 Control Register 1
0462	VPA_ANA_CON0	16	VPA_ANA Control Register 0
0464	VPA_ANA_CON1	16	VPA_ANA Control Register 1
0466	VPA_ANA_CON2	16	VPA_ANA Control Register 2
0468	VPA_ANA_CON3	16	VPA_ANA Control Register 3
046A	VLTE_ANA_CON0	16	VLTE_ANA Control Register 0
046C	VLTE_ANA_CON1	16	VLTE_ANA Control Register 1
046E	VLTE_ANA_CON2	16	VLTE_ANA Control Register 2
0470	VLTE_ANA_CON3	16	VLTE_ANA Control Register 3
0472	VLTE_ANA_CON4	16	VLTE_ANA Control Register 4
048A	VPROC_CON11	16	VPROC Control Register 11
04B2	VSRAM_CON11	16	VSRAM Control Register 11
04DA	VLTE_CON11	16	VLTE Control Register 11
0616	VCORE1_CON11	16	VCORE1 Control Register 11
063E	VSYS22_CON11	16	VSYS22 Control Register 11
0666	VPA_CON11	16	VPA Control Register 11
0800	ZCD_CON0	16	ZCD Control Register 0
0802	ZCD_CON1	16	ZCD Control Register 1
0804	ZCD_CON2	16	ZCD Control Register 2
0806	ZCD_CON3	16	ZCD Control Register 3
0808	ZCD_CON4	16	ZCD Control Register 4
080A	ZCD_CON5	16	ZCD Control Register 5
080C	ISINK0_CON0	16	ISINK0 Control Register 0
080E	ISINK0_CON1	16	ISINK0 Control Register 1
0810	ISINK0_CON2	16	ISINK0 Control Register 2
0812	ISINK0_CON3	16	ISINK0 Control Register 3
0814	ISINK1_CON0	16	ISINK1 Control Register 0

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Address	Name	Width	Register Function
0816	ISINK1_CON1	16	ISINK1 Control Register 1
0818	ISINK1_CON2	16	ISINK1 Control Register 2
081A	ISINK1_CON3	16	ISINK1 Control Register 3
081C	ISINK2_CON1	16	ISINK2 Control Register 1
081E	ISINK3_CON1	16	ISINK3 Control Register 1
0824	ISINK_PHASE_DLY	16	ISINK PHASE DELAY
0826	ISINK_SFSTR	16	ISINK Soft Start
0828	ISINK_EN_CTRL	16	ISINK Enable Control
082A	ISINK_MODE_CTRL	16	ISINK Mode Control
0A00	VTCXO_0_CON0	16	VTCXO_0 Control Register 0
0A02	VTCXO_1_CON0	16	VTCOX_1 Control Register 0
0A04	VAUD28_CON0	16	VAUD28 Control Register 0
0A06	VAUX18_CON0	16	VAUX18 Control Register 0
0A08	VRF18_0_CON0	16	VRF18_0 Control Register 0
0A0A	VRF18_0_CON1	16	VRF18_0 Control Register 1
0A0C	VCAMA_CON0	16	VCAMA Control Register 0
0A0E	VCN28_CON0	16	VCN28 Control Register 0
0A10	VCN33_CON0	16	VCN33 Control Register 0
0A12	VCN33_CON1	16	VCN33 Control Register 1
0A14	VCN33_CON2	16	VCN33 Control Register 2
0A16	VRF18_1_CON0	16	VRF18_1 Control Register 0
0A18	VRF18_1_CON1	16	VRF18_1 Control Register 1
0A1A	VUSB33_CON0	16	USB33 Control Register 0
0A1C	VMCH_CON0	16	VMCH Control Register 0
0A1E	VMCH_CON1	16	VMCH Control Register 1
0A20	VMC_CON0	16	VMC Control Register 0
0A22	VMC_CON1	16	VMC control register 1
0A24	VEMC_3V3_CON0	16	VEMC_3V3 Control Register 0
0A26	VEMC_3V3_CON1	16	VEMC_3V3 Control Register 1
0A28	VIO28_CON0	16	VIO28 Control Register 0
0A2A	VCAMAF_CON0	16	VCAMAF Control Register 0
0A2C	VGP1_CON0	16	VGP1 Control Register 0
0A2E	VGP1_CON1	16	VGP1 Control Register 1
0A30	VEFUSE_CON0	16	VEFUSE Control Register 0
0A32	VSIM1_CON0	16	VSIM1 Control Register 0
0A34	VSIM2_CON0	16	VSIM2 Control Register 0
0A36	VIO18_CON0	16	VIO18 Control Register 0

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Address	Name	Width	Register Function
0A38	VIBR_CON0	16	VIBR Control Register 0
0A3A	VCN18_CON0	16	VCN18 Control Register 0
0A3C	VCAM_CON0	16	VCMAD Control Register 0
0A3E	VCAMIO_CON0	16	VCAMIO Control Register 0
0A40	LDO_VSRAM_CON0	16	LDO_VSRAM Control Register 0
0A42	LDO_VSRAM_CON1	16	LDO_VSRAM Control Register 1
0A44	VTREF_CON0	16	VTREF Control Register 0
0A46	VM_CON0	16	VM Control Register 0
0A48	VM_CON1	16	VM Control Register 1
0A4A	VRTC_CON0	16	VRTC Control Register 0
0A4E	ALDO_ANA_CON0	16	ADLDO Control Register 0
0A50	ADLDO_ANA_CON1	16	ADLDO Control Register 1
0A52	ADLDO_ANA_CON2	16	ADLDO Control Register 2
0A54	ADLDO_ANA_CON3	16	ADLDO Control Register 3
0A56	ADLDO_ANA_CON4	16	ADLDO Control Register 4
0A58	ADLDO_ANA_CON5	16	ADLDO Control Register 5
0A5A	ADLDO_ANA_CON6	16	ADLDO Control Register 6
0A5C	ADLDO_ANA_CON7	16	ADLDO Control Register 7
0A5E	ADLDO_ANA_CON8	16	ADLDO Control Register 8
0A60	ADLDO_ANA_CON9	16	ADLDO Control Register 9
0A62	ADLDO_ANA_CON10	16	ADLDO Control Register 10
0A64	ADLDO_ANA_CON11	16	ADLDO Control Register 11
0A66	ADLDO_ANA_CON12	16	ADLDO Control Register 12
0A68	ADLDO_ANA_CON13	16	ADLDO Control Register 13
0A6A	DLDO_ANA_CON0	16	DLDO Control Register 0
0A6C	DLDO_ANA_CON1	16	DLDO Control Register 1
0A6E	DLDO_ANA_CON2	16	DLDO Control Register 2
0A70	DLDO_ANA_CON3	16	DLDO Control Register 3
0A72	DLDO_ANA_CON4	16	DLDO Control Register 4
0A74	DLDO_ANA_CON5	16	DLDO Control Register 5

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Address	Name	Width	Register Function
0A76	SLDO_ANA_CON0	16	SLDO Control Register 0
0A78	SLDO_ANA_CON1	16	SLDO Control Register 1
0A7A	SLDO_ANA_CON2	16	SLDO Control Register 2
0A7C	SLDO_ANA_CON3	16	SLDO Control Register 3
0A7E	SLDO_ANA_CON4	16	SLDO Control Register 4
0A80	SLDO_ANA_CON5	16	SLDO Control Register 5
0A82	SLDO_ANA_CON6	16	SLDO Control Register 6
0A84	SLDO_ANA_CON7	16	SLDO Control Register 7
0A86	SLDO_ANA_CON8	16	SLDO Control Register 8
0A88	SLDO_ANA_CON9	16	SLDO Control Register 9
0A8A	SLDO_ANA_CON10	16	SLDO Control Register10
0A90	SPK_CON0	16	Speaker Control Register 0
0A92	SPK_CON1	16	Speaker Control Register 1
0A94	SPK_CON2	16	Speaker Control Register 2
0A9C	SPK_CON6	16	Speaker Control Register 6
0A9E	SPK_CON7	16	Speaker Control Register 7
0AA0	SPK_CON8	16	Speaker Control Register 8
0AA2	SPK_CON9	16	Speaker Control Register 9
0AA4	SPK_CON10	16	Speaker Control Register 10
0AA6	SPK_CON11	16	Speaker Control Register 11
0AA8	SPK_CON12	16	Speaker Control Register 12
0AAA	SPK_CON13	16	Speaker Control Register 13
0AAC	SPK_CON14	16	Speaker Control Register 14
0AAE	SPK_CON15	16	Speaker Control Register 15
0AB0	SPK_CON16	16	Speaker Control Register 16
0AB2	SPK_ANA_CON0	16	SPK Control Register 0
0AB4	SPK_ANA_CON1	16	SPK Control Register 1
0AB6	SPK_ANA_CON3	16	SPK Control Register 3
0C00	OTP_CON0	16	OTP Control Register 0
0C02	OTP_CON1	16	OTP Control Register 1
0C04	OTP_CON2	16	OTP Control Register 2
0C06	OTP_CON3	16	OTP Control Register 3
0C08	OTP_CON4	16	OTP Control Register 4
0C0A	OTP_CON5	16	OTP Control Register 5
0C0C	OTP_CON6	16	OTP Control Register 6

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Address	Name	Width	Register Function
0C0E	OTP_CON7	16	OTP Control Register 7
0C10	OTP_CON8	16	OTP Control Register 8
0C12	OTP_CON9	16	OTP Control Register 9
0C14	OTP_CON10	16	OTP Control Register 10
0C16	OTP_CON11	16	OTP Control Register 11
0C18	OTP_CON12	16	OTP Control Register 12
0C1A	OTP_CON13	16	OTP Control Register 13
0C1C	OTP_CON14	16	OTP Control Register 14
0C1E	OTP_DOUT_0_15	16	OTP dout 0 15
0C20	OTP_DOUT_16_31	16	OTP dout 16 31
0C22	OTP_DOUT_32_47	16	OTP dout 32 47
0C24	OTP_DOUT_48_63	16	OTP dout 48 63
0C26	OTP_DOUT_64_79	16	OTP dout 64 79
0C28	OTP_DOUT_80_95	16	OTP dout 80 95
0C2A	OTP_DOUT_96_111	16	OTP dout 96 111
0C2C	OTP_DOUT_112_127	16	OTP dout 112 127
0C2E	OTP_DOUT_128_143	16	OTP dout 128 143
0C30	OTP_DOUT_144_159	16	OTP dout 144 159
0C32	OTP_DOUT_160_175	16	OTP dout 160 175
0C34	OTP_DOUT_176_191	16	OTP dout 176 191
0C36	OTP_DOUT_192_207	16	OTP dout 192 207
0C38	OTP_DOUT_208_223	16	OTP dout 208 223
0C3A	OTP_DOUT_224_239	16	OTP dout 224 239
0C3C	OTP_DOUT_240_255	16	OTP dout 240 255
0C3E	OTP_DOUT_256_271	16	OTP dout 256 271
0C40	OTP_DOUT_272_287	16	OTP dout 272 287
0C42	OTP_DOUT_288_303	16	OTP dout 288 303
0C44	OTP_DOUT_304_319	16	OTP dout 304 319
0C46	OTP_DOUT_320_335	16	OTP dout 320 335
0C48	OTP_DOUT_336_351	16	OTP dout 336 351

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Address	Name	Width	Register Function
0C4A	OTP_DOUT_352_367	16	OTP dout 352 367
0C4C	OTP_DOUT_368_383	16	OTP dout 368 383
0C4E	OTP_DOUT_384_399	16	OTP dout 384 399
0C50	OTP_DOUT_400_415	16	OTP dout 400 415
0C52	OTP_DOUT_416_431	16	OTP dout 416 431
0C54	OTP_DOUT_432_447	16	OTP dout 432 447
0C56	OTP_DOUT_448_463	16	OTP dout 448 463
0C58	OTP_DOUT_464_479	16	OTP dout 464 479
0C5A	OTP_DOUT_480_495	16	OTP dout 480 495
0C5C	OTP_DOUT_496_511	16	OTP dout 496 511
0C5E	OTP_VAL_0_15	16	OTP val 0 15
0C60	OTP_VAL_16_31	16	OTP val 16 31
0C62	OTP_VAL_32_47	16	OTP val 32 47
0C64	OTP_VAL_48_63	16	OTP val 48 63
0C66	OTP_VAL_64_79	16	OTP val 64 79
0C68	OTP_VAL_80_95	16	OTP val 80 95
0C6A	OTP_VAL_96_111	16	OTP val 96 111
0C6C	OTP_VAL_112_127	16	OTP val 112 127
0C6E	OTP_VAL_128_143	16	OTP val 128 143
0C70	OTP_VAL_144_159	16	OTP val 144 159
0C72	OTP_VAL_160_175	16	OTP val 160 175
0C74	OTP_VAL_176_191	16	OTP val 176 191
0C76	OTP_VAL_192_207	16	OTP val 192 207
0C78	OTP_VAL_208_223	16	OTP val 208 223
0C7A	OTP_VAL_224_239	16	OTP val 224 239
0C7C	OTP_VAL_240_255	16	OTP val 240 255
0C7E	OTP_VAL_256_271	16	OTP val 256 271

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Address	Name	Width	Register Function
0C80	OTP_VAL_272_287	16	OTP val 272 287
0C82	OTP_VAL_288_303	16	OTP val 288 303
0C84	OTP_VAL_304_319	16	OTP val 304 319
0C86	OTP_VAL_320_335	16	OTP val 320 335
0C88	OTP_VAL_336_351	16	OTP val 336 351
0C8A	OTP_VAL_352_367	16	OTP val 352 367
0C8C	OTP_VAL_368_383	16	OTP val 368 383
0C8E	OTP_VAL_384_399	16	OTP val 384 399
0C90	OTP_VAL_400_415	16	OTP val 400 415
0C92	OTP_VAL_416_431	16	OTP val 416 431
0C94	OTP_VAL_432_447	16	OTP val 432 447
0C96	OTP_VAL_448_463	16	OTP val 448 463
0C98	OTP_VAL_464_479	16	OTP val 464 479
0C9A	OTP_VAL_480_495	16	OTP val 480 495
0C9C	OTP_VAL_496_511	16	OTP val 496 511
0CA6	FGADC_CON1	16	FGADC Control Register 1
0CA8	FGADC_CON2	16	FGADC Control Register 2
0CAA	FGADC_CON3	16	FGADC Control Register 3
0CAC	FGADC_CON4	16	FGADC Control Register 4
0CB2	FGADC_CON7	16	FGADC Control Register 7
0CB8	FGADC_CON10	16	FGADC Control Register 10
0CDC	AUDDEC_ANA_CON0	16	AUDDEC Control Register 0
0CDE	AUDDEC_ANA_CON1	16	AUDDEC Control Register 1
0CE0	AUDDEC_ANA_CON2	16	AUDDEC Control Register 2
0CE2	AUDDEC_ANA_CON3	16	AUDDEC Control Register 3
0CE4	AUDDEC_ANA_CON4	16	AUDDEC Control Register 4
0CE6	AUDDEC_ANA_CON5	16	AUDDEC Control Register 5
0CE8	AUDDEC_ANA_CON6	16	AUDDEC Control Register 6
0CEA	AUDDEC_ANA_CON7	16	AUDDEC Control Register 7
0CEC	AUDDEC_ANA	16	AUDDEC Control Register 8

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Address	Name	Width	Register Function
	_CON8		
0CEE	AUDENC_ANA_CON0	16	AUDENC Control Register 0
0CF0	AUDENC_ANA_CON1	16	AUDENC Control Register 1
0CF2	AUDENC_ANA_CON2	16	AUDENC Control Register 2
0CF4	AUDENC_ANA_CON3	16	AUDENC Control Register 3
0CF6	AUDENC_ANA_CON4	16	AUDENC Control Register 4
0CF8	AUDENC_ANA_CON5	16	AUDENC Control Register 5
0CFA	AUDENC_ANA_CON6	16	AUDENC Control Register 6
0CFC	AUDENC_ANA_CON7	16	AUDENC Control Register 7
0CFE	AUDENC_ANA_CON8	16	AUDENC Control Register 8
0D00	AUDENC_ANA_CON9	16	AUDENC Control Register 9
0D02	AUDENC_ANA_CON10	16	AUDENC Control Register 10
0D04	AUDNCP_CLKDIV_CON0	16	AUDNCP_CLKDIV Control Register 0
0D06	AUDNCP_CLKDIV_CON1	16	AUDNCP_CLKDIV Control Register 1
0D08	AUDNCP_CLKDIV_CON2	16	AUDNCP_CLKDIV Control Register 2
0D0A	AUDNCP_CLKDIV_CON3	16	AUDNCP_CLKDIV Control Register 3
0D0C	AUDNCP_CLKDIV_CON4	16	AUDNCP_CLKDIV Control Register 4
0E00	AUXADC_ADC0	16	AUXADC ADC Register 0
0E02	AUXADC_ADC1	16	AUXADC ADC Register 1
0E04	AUXADC_ADC2	16	AUXADC ADC Register 2
0E06	AUXADC_ADC3	16	AUXADC ADC Register 3
0E08	AUXADC_ADC4	16	AUXADC ADC Register 4
0E0A	AUXADC_ADC5	16	AUXADC ADC Register 5
0E0C	AUXADC_ADC6	16	AUXADC ADC Register 6
0E0E	AUXADC_ADC7	16	AUXADC ADC Register 7
0E10	AUXADC_ADC8	16	AUXADC ADC Register 8
0E12	AUXADC_ADC9	16	AUXADC ADC Register 9
0E14	AUXADC_ADC10	16	AUXADC ADC Register 10

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Address	Name	Width	Register Function
0E16	AUXADC_ADC11	16	AUXADC ADC Register 11
0E18	AUXADC_ADC12	16	AUXADC ADC Register 12
0E1A	AUXADC_ADC13	16	AUXADC ADC Register 13
0E1C	AUXADC_ADC14	16	AUXADC ADC Register 14
0E1E	AUXADC_ADC15	16	AUXADC ADC Register 15
0E20	AUXADC_ADC16	16	AUXADC ADC Register 16
0E22	AUXADC_ADC17	16	AUXADC ADC Register 17
0E24	AUXADC_ADC18	16	AUXADC ADC Register 18
0E26	AUXADC_ADC19	16	AUXADC ADC Register 19
0E28	AUXADC_ADC20	16	AUXADC ADC Register 20
0E2A	AUXADC_ADC21	16	AUXADC ADC Register 21
0E2C	AUXADC_ADC22	16	AUXADC ADC Register 22
0E2E	AUXADC_ADC23	16	AUXADC ADC Register 23
0E30	AUXADC_ADC24	16	AUXADC ADC Register 24
0E32	AUXADC_ADC25	16	AUXADC ADC Register 25
0E34	AUXADC_ADC26	16	AUXADC ADC Register 26
0E36	AUXADC_ADC27	16	AUXADC ADC Register 27
0E38	AUXADC_ADC28	16	AUXADC ADC Register 28
0E3A	AUXADC_ADC29	16	AUXADC ADC Register 29
0E3C	AUXADC_ADC30	16	AUXADC ADC Register 30
0E3E	AUXADC_ADC31	16	AUXADC ADC Register 31
0E40	AUXADC_ADC32	16	AUXADC ADC Register 32
0E42	AUXADC_ADC33	16	AUXADC ADC Register 33
0E44	AUXADC_BUF0	16	AUXADC_BUF0
0E46	AUXADC_BUF1	16	AUXADC_BUF1
0E48	AUXADC_BUF2	16	AUXADC_BUF2
0E4A	AUXADC_BUF3	16	AUXADC_BUF3
0E4C	AUXADC_BUF	16	AUXADC_BUF4

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Address	Name	Width	Register Function
	4		
0E4E	**AUXADC_BUF5**	16	AUXADC_BUF5
0E50	**AUXADC_BUF6**	16	AUXADC_BUF6
0E52	**AUXADC_BUF7**	16	AUXADC_BUF7
0E54	**AUXADC_BUF8**	16	AUXADC_BUF8
0E56	**AUXADC_BUF9**	16	AUXADC_BUF9
0E58	**AUXADC_BUF10**	16	AUXADC_BUF10
0E5A	**AUXADC_BUF11**	16	AUXADC_BUF11
0E5C	**AUXADC_BUF12**	16	AUXADC_BUF12
0E5E	**AUXADC_BUF13**	16	AUXADC_BUF13
0E60	**AUXADC_BUF14**	16	AUXADC_BUF14
0E62	**AUXADC_BUF15**	16	AUXADC_BUF15
0E64	**AUXADC_BUF16**	16	AUXADC_BUF16
0E66	**AUXADC_BUF17**	16	AUXADC_BUF17
0E68	**AUXADC_BUF18**	16	AUXADC_BUF18
0E6A	**AUXADC_BUF19**	16	AUXADC_BUF19
0E6C	**AUXADC_BUF20**	16	AUXADC_BUF20
0E6E	**AUXADC_BUF21**	16	AUXADC_BUF21
0E70	**AUXADC_BUF22**	16	AUXADC_BUF22
0E72	**AUXADC_BUF23**	16	AUXADC_BUF23
0E74	**AUXADC_BUF24**	16	AUXADC_BUF24
0E76	**AUXADC_BUF25**	16	AUXADC_BUF25
0E78	**AUXADC_BUF26**	16	AUXADC_BUF26
0E7A	**AUXADC_BUF27**	16	AUXADC_BUF27
0E7C	**AUXADC_BUF28**	16	AUXADC_BUF28
0E7E	**AUXADC_BUF29**	16	AUXADC_BUF29
0E80	**AUXADC_BUF30**	16	AUXADC_BUF30
0E82	**AUXADC_BUF31**	16	AUXADC_BUF31

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Address	Name	Width	Register Function
0E84	AUXADC_STA0	16	AUXADC_STA0
0E86	AUXADC_STA1	16	AUXADC_STA1
0EF4	AUXADC_VISMPS0_5	16	AUXADC_VISMPS0_5
0F02	AUXADC_LBAT2_5	16	AUXADC_LBAT2_5
0F14	ACCDET_CON0	16	ACCDET Control Register 0
0F16	ACCDET_CON1	16	ACCDET Control Register 1
0F18	ACCDET_CON2	16	ACCDET control register 2
0F1A	ACCDET_CON3	16	ACCDET Control Register 3
0F1C	ACCDET_CON4	16	ACCDET Control Register 4
0F1E	ACCDET_CON5	16	ACCDET Control Register 5
0F20	ACCDET_CON6	16	ACCDET Control Register 6
0F22	ACCDET_CON7	16	ACCDET Control Register 7
0F24	ACCDET_CON8	16	ACCDET Control Register 8
0F26	ACCDET_CON9	16	ACCDET Control Register 9
0F28	ACCDET_CON10	16	ACCDET Control Register 10
0F2C	ACCDET_CON12	16	ACCDET Control Register 12
0F30	ACCDET_CON14	16	ACCDET Control Register 14
0F32	ACCDET_CON15	16	ACCDET Control Register 15
0F34	ACCDET_CON16	16	ACCDET Control Register 16
0F3A	ACCDET_CON19	16	ACCDET Control Register 19
0F48	CHR_CON0	16	Charger Control Register 0
0F4A	CHR_CON1	16	Charger Control Register 1
0F4C	CHR_CON2	16	Charger Control Register 2
0F4E	CHR_CON3	16	Charger Control Register 3
0F50	CHR_CON4	16	Charger Control Register 4
0F54	CHR_CON6	16	Charger Control Register 6
0F56	CHR_CON7	16	Charger Control Register 7
0F5A	CHR_CON9	16	Charger Control Register 9
0F5C	CHR_CON10	16	Charger Control Register 10
0F60	CHR_CON12	16	Charger Control Register 12
0F62	CHR_CON13	16	Charger Control Register 13
0F64	CHR_CON14	16	Charger Control Register 14
0F66	CHR_CON15	16	Charger Control Register 15
0F68	CHR_CON16	16	Charger Control Register 16
0F6A	CHR_CON17	16	Charger Control Register 17
0F6C	CHR_CON18	16	Charger Control Register 18
0F6E	CHR_CON19	16	Charger Control Register 19
0F70	CHR_CON20	16	Charger Control Register 20
0F72	CHR_CON21	16	Charger Control Register 21

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Address	Name	Width	Register Function
0F74	CHR_CON22	16	Charger Control Register 22
0F76	CHR_CON23	16	Charger Control Register 23
0F78	CHR_CON24	16	Charger Control Register 24
0F7A	CHR_CON25	16	Charger Control Register 25
0F7C	CHR_CON26	16	Charger Control Register 26
0F7E	CHR_CON27	16	Charger Control Register 27
0F80	CHR_CON28	16	Charger Control Register 28
0F82	CHR_CON29	16	Charger Control Register 29
0F84	CHR_CON30	16	Charger Control Register 30
0F86	CHR_CON31	16	Charger Control Register 31
0F88	CHR_CON32	16	Charger Control Register 32
0F8A	CHR_CON33	16	Charger Control Register 33
0F8C	CHR_CON34	16	Charger Control Register 34
0F8E	CHR_CON35	16	Charger Control Register 35
0F90	CHR_CON36	16	Charger Control Register 36
0F92	CHR_CON37	16	Charger Control Register 37
0F94	CHR_CON38	16	Charger Control Register 38
0F96	CHR_CON39	16	Charger Control Register 39
0F98	CHR_CON40	16	Charger Control Register 40
0F9A	CHR_CON41	16	Charger Control Register 41
0F9C	CHR_CON42	16	Charger Control Register 42
0F9E	BATON_CON0	16	BATON Control Register 0
0FA0	CHR_CON43	16	Charger Control Register 43

0000 STRUP_CON0 STRUP Control Register 0 0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											THR_HWPDN_EN					THR_DET_DIS
Type											RW					RW
Reset											0					0

Bit(s)	Name	Description
5	THR_HWPDN_EN	**Enables thermal auto power-down** Powers down some PMU modules 0: Disable 1: Enable
0	THR_DET_DIS	**Disables thermal detection function and thermal shut-down** 0: Normal mode 1: Disable thermal detection

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0002 **STRUP_CON2** **STRUP Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_STRUP_IREF_TRIM				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RG_STRUP_IREF_TRIM	**Reference current trimming bits** Trimming current range: 0.5uA~1.4375uA (step=31.25nA), typ=1uA 00000: 1uA 00001~01111: +31.25nA/step 10000: 0.5uA 10001~11111: -31.25nA/step

0004 **STRUP_CON3** **STRUP Control Register 3** **4001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_VREF_BG												RG_FCHR_PU_EN	RG_FCHR_KEYDET_EN	
Type		RW												RW	RW	
Reset		1	0	0										0	0	

Bit(s)	Name	Description
14:12	RG_VREF_BG	**Reference current fine tuning to compensate bandgap (BG) voltage variation** 000: VBG=1.16V 001: VBG=1.17V 010: VBG=1.18V 011: VBG=1.19V 100: VBG=1.20V (default) 101: VBG=1.21V 110: VBG=1.22V 111: VBG=1.23V
2	RG_FCHR_PU_EN	**Enables FCHR internal resistor pull-up** 0: Disable pull up R 1: Enable pull up R
1	RG_FCHR_KEYDET_EN	**FCHR mode state hold without key press detection feature** 0: Disable 1: Enable

0008 **STRUP_CON5** **STRUP Control Register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						PMU_THR_STATUS										
Type						RO										

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Reset						0	0	0								

Bit(s)	Name	Description
10:8	PMU_THR_STATUS	Thermal detection status

0010 **STRUP_CON9** **STRUP Control Register 9** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_OSC_EN	JUST_PWRKEY_RST														
Type	RO	RO														
Reset	0	0														

Bit(s)	Name	Description
15	QI_OSC_EN	**Enables internal oscillator** 0: Disable 1: Enable
14	JUST_PWRKEY_RST	**Long pressed reset indicator**

0012 **STRUP_CON10** **STRUP control register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															STRUP_EXT_PMIC_SEL	STRUP_EXT_PMIC_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	STRUP_EXT_PMIC_SEL	**Selects QI_EXT_PMIC_EN control** 0: HW mode 1: SW mode
0	STRUP_EXT_PMIC_EN	**Enables QI_EXT_PMIC_EN software mode**

0014 **STRUP_CON11** **STRUP Control Register 11** **0020**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									STR	STR	STR	STR				

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									UP_AUXADC_RSTB_SEL	UP_AUXADC_START_SEL	UP_AUXADC_RSTB_SW	UP_AUXADC_START_SW				
Type									RW	RW	RW	RW				
Reset									0	0	1	0				

Bit(s)	Name	Description
7	STRUP_AUXADC_RSTB_SEL	**Selects STRUP_AUXADC_RSTB** 0: HW mode 1: SW mode
6	STRUP_AUXADC_START_SEL	**Selects STRUP_AUXADC_START** 0: HW mode 1: SW mode
5	STRUP_AUXADC_RSTB_SW	**STRUP_AUXADC_RSTB SW path**
4	STRUP_AUXADC_START_SW	**STRUP_AUXADC_START SW path**

0018 **STRUP_CON13** **STRUP Control Register 13** **17C0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_UVLO_VTHL_RSV0															
Type	RW															
Reset	0	0	0	1	0											

Bit(s)	Name	Description
15:11	RG_UVLO_VTHL_RSV0	**Selects UVLO low threshold** 00000: 2.5V 00001: 2.55V 00010: 2.6V (default) 00011: 2.65V 00100: 2.7V 00101: 2.75V 00110: 2.8V 00111: 2.85V 01000: 2.9V

001A **STRUP_CON14** **STRUP Control Register 14** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_BGR_RSV0	RG_BGR_RSV1	RG_BGR_RSV2			RG_BGR_RSV3	RG_BGR_RSV4								RG_BGR_RSV5	RG_BGR_RSV6
Type	RW	RW	RW			RW	RW								RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0				0	0

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Bit(s)	Name	Description
15	RG_BGR_RSV0	
14	RG_BGR_RSV1	
13:11	RG_BGR_RSV2	
10	RG_BGR_RSV3	
9:5	RG_BGR_RSV4	
1	RG_BGR_RSV5	
0	RG_BGR_RSV6	

001C **STRUP_CON15** **STRUP Control Register 15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_STRUP_RSV							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RG_STRUP_RSV	

001E **STRUP_CON16** **STRUP Control Register 16** **0800**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STRUP_DIG0_RSV1				RG_TESTMODE_SWEN								RG_EN_E4	RG_EN_E8	RG_EN_SR	RG_EN_SMT
Type	RW				RW								RW	RW	RW	RW
Reset	0	0	0	0	1								0	0	0	0

Bit(s)	Name	Description
15:12	STRUP_DIG0_RSV1	
11	RG_TESTMODE_SWEN	
3	RG_EN_E4	
2	RG_EN_E8	
1	RG_EN_SR	
0	RG_EN_SMT	

0040 **STRUP_ANA_CON0** **STRUP ANA Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_												

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				RST_DRVSEL												
Type				RW												
Reset				0												

Bit(s)	Name	Description
12	RG_RST_DRVSEL	**Reset pin output driving capability Selection** 0: 7.5mA (default) 1: 15mA

0206 **TEST_OUT** **TEST_OUT** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TEST_OUT							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	TEST_OUT	Monitor

0220 **TOPSTATUS** **TOP Status** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														HOMEKEY_DEB	PWRKEY_DEB	
Type														RO	RO	
Reset														0	0	

Bit(s)	Name	Description
2	HOMEKEY_DEB	
1	PWRKEY_DEB	

0222 **TDSEL_CON** **TDSEL_CON** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_E32CAL_TDSEL	RG_AUD_TDSEL	RG_SPI_TDSEL	RG_PMU_TDSEL
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	RG_E32CAL_TDSEL	TDSEL

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Bit(s)	Name	Description
2	RG_AUD_TDSEL	TDSEL
1	RG_SPI_TDSEL	TDSEL
0	RG_PMU_TDSEL	TDSEL

0224 **RDSEL_CON** **RDSEL_CON** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_E32CAL_RDSEL	RG_AUD_RDSEL	RG_SPI_RDSEL	RG_PMU_RDSEL
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	RG_E32CAL_RDSEL	**RDSEL**
2	RG_AUD_RDSEL	**RDSEL**
1	RG_SPI_RDSEL	**RDSEL**
0	RG_PMU_RDSEL	**RDSEL**

0226 **SMT_CON0** **SMT_CON0** **003C**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_SMT_RTC_32K1V8_1	RG_SMT_RTC_32K1V8_0	RG_SMT_SRCLKEN_IN1	RG_SMT_SRCLKEN_IN0	RG_SMT_HOMEKEY	RG_SMT_WDTRSTB_IN
Type											RW	RW	RW	RW	RW	RW
Reset											1	1	1	1	0	0

Bit(s)	Name	Description
5	RG_SMT_RTC_32K1V8_1	**SMT** 0: Disable 1: Enable
4	RG_SMT_RTC_32K1V8_0	**SMT** 0: Disable 1: Enable
3	RG_SMT_SRCLKEN_IN1	**SMT** 0: Disable 1: Enable
2	RG_SMT_SRCLKEN_IN0	**SMT** 0: Disable 1: Enable
1	RG_SMT_HOMEKEY	**SMT** 0: Disable 1: Enable

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Bit(s)	Name	Description
0	RG_SMT_WDTRSTB_IN	**SMT** 0: Disable 1: Enable

0228 **SMT_CON1** **SMT_CON1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_SMT_SPI_MISO	RG_SMT_SPI_MOSI	RG_SMT_SPI_CSN	RG_SMT_SPI_CLK
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	RG_SMT_SPI_MISO	**SMT** 0: Disable 1: Enable
2	RG_SMT_SPI_MOSI	**SMT** 0: Disable 1: Enable
1	RG_SMT_SPI_CSN	**SMT** 0: Disable 1: Enable
0	RG_SMT_SPI_CLK	**SMT** 0: Disable 1: Enable

022A **SMT_CON2** **SMT_CON2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_SMT_XOSC_EN	RG_SMT_ENBB		RG_SMT_AUD_DAT_MISO	RG_SMT_AUD_DAT_MOSI	RG_SMT_AUD_CLK
Type											RW	RW		RW	RW	RW
Reset											0	0		0	0	0

Bit(s)	Name	Description
5	RG_SMT_XOSC_EN	**SMT** 0: Disable 1: Enable
4	RG_SMT_ENBB	**SMT** 0: Disable 1: Enable
2	RG_SMT_AUD_DAT_MISO	**SMT** 0: Disable

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Bit(s)	Name	Description
		1: Enable
1	RG_SMT_AUD_DAT_MOSI	**SMT** 0: Disable 1: Enable
0	RG_SMT_AUD_CLK	**SMT** 0: Disable 1: Enable

022C **DRV_CON0** **DRV_CON0** **CCCC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OCTL_RTC_32K1V8_1				RG_OCTL_RTC_32K1V8_0				RG_OCTL_SRCLKEN_IN1				RG_OCTL_SRCLKEN_IN0			
Type	RW				RW				RW				RW			
Reset	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0

Bit(s)	Name	Description
15:12	RG_OCTL_RTC_32K1V8_1	OC CTL
11:8	RG_OCTL_RTC_32K1V8_0	OC CTL
7:4	RG_OCTL_SRCLKEN_IN1	OC CTL
3:0	RG_OCTL_SRCLKEN_IN0	OC CTL

022E **DRV_CON1** **DRV_CON1** **CCCC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OCTL_SPI_MISO				RG_OCTL_SPI_MOSI				RG_OCTL_SPI_CSN				RG_OCTL_SPI_CLK			
Type	RW				RW				RW				RW			
Reset	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0

Bit(s)	Name	Description
15:12	RG_OCTL_SPI_MISO	OC CTL
11:8	RG_OCTL_SPI_MOSI	OC CTL
7:4	RG_OCTL_SPI_CSN	OC CTL
3:0	RG_OCTL_SPI_CLK	OC CTL

0230 **DRV_CON2** **DRV_CON2** **0CCC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_OCTL_AUD_CLK				RG_OCTL_AUD_DAT_MISO				RG_OCTL_AUD_DAT_MOSI			

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Type					RW				RW				RW			
Reset					1	1	0	0	1	1	0	0	1	1	0	0

Bit(s)	Name	Description
11:8	RG_OCTL_AUD_CLK	**OC CTL**
7:4	RG_OCTL_AUD_DAT_MISO	**OC CTL**
3:0	RG_OCTL_AUD_DAT_MOSI	**OC CTL**

0232 DRV_CON3 DRV_CON3 0CCC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_OCTL_XOSC_EN				RG_OCTL_ENBB				RG_OCTL_HOMEKEY			
Type					RW				RW				RW			
Reset					1	1	0	0	1	1	0	0	1	1	0	0

Bit(s)	Name	Description
11:8	RG_OCTL_XOSC_EN	OC CTL
7:4	RG_OCTL_ENBB	OC CTL
3:0	RG_OCTL_HOMEKEY	OC CTL

0234 TOP_STATUS TOP_STATUS 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TOP_STATUS			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	TOP_STATUS	

023A RGS_ANA_MON RGS_ANA_MON 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RGS_VSYS22_ENPWM_STATUS	RGS_VCORE1_ENPWM_STATUS	RGS_VLTE_ENPWM_STATUS	RGS_VPROC_ENPWM_STATUS
Type													RO	RO	RO	RO
Reset													0	0	0	0

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Bit(s)	Name	Description
3	RGS_VSYS22_ENPWM_STATUS	**ENPWM status** H: PWM mode L: PFM mode
2	RGS_VCORE1_ENPWM_STATUS	
1	RGS_VLTE_ENPWM_STATUS	
0	RGS_VPROC_ENPWM_STATUS	**ENPWM status** H: PWM mode L: PFM mode

023C **TOP_CKPDN_CON0** **TOP_CKPDN Control Register 0** **DEFC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_ZCD13M_CK_PDN**	**RG_AUD_CK_PDN**	**RG_AUDIF_CK_PDN**	**RG_AUDNCP_CK_PDN**	**RG_AUXADC_26M_CK_PDN**	**RG_AUXADC_RNG_CK_PDN**	**RG_AUXADC_SMPS_CK_PDN**	**RG_AUXADC_1M_CK_PDN**	**RG_DRV_ISINK3_CK_PDN**	**RG_DRV_ISINK2_CK_PDN**	**RG_DRV_ISINK1_CK_PDN**	**RG_DRV_ISINK0_CK_PDN**	**RG_DRV_32K_CK_PDN**	**RG_DRV_2M_CK_PDN**	**RG_SMPS_AUD_CK_PDN**	**RG_SMPS_PD_CK_PDN**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	0	1	1	1	1	0	1	1	1	1	1	1	0	0

Bit(s)	Name	Description
15	RG_ZCD13M_CK_PDN	**Powers down ZCD13M_CK** 0: Power on 1: Power down
14	RG_AUD_CK_PDN	**Powers down AUD_CK** 0: Power on 1: Power down
13	RG_AUDIF_CK_PDN	**Powers down AUDIF_CK** 0: Power on 1: Power down
12	RG_AUDNCP_CK_PDN	**Powers down AUDNCP_CK** 0: Power on 1: Power down
11	RG_AUXADC_26M_CK_PDN	**Powers down AUXADC_26M_CK** 0: Power on 1: Power down
10	RG_AUXADC_RNG_CK_PDN	**Powers down AUXADC_RNG_CK** 0: Power on 1: Power down
9	RG_AUXADC_SMPS_CK_PDN	**Powers down AUXADC_SMPS_CK** 0: Power on 1: Power down
8	RG_AUXADC_1M_CK_PDN	**Powers down AUXADC_1M_CK** 0: Power on 1: Power down

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Bit(s)	Name	Description
7	RG_DRV_ISINK3_CK_PDN	**Powers down DRV_ISINK3_CK** 0: Power on 1: Power down
6	RG_DRV_ISINK2_CK_PDN	**Powers down DRV_ISINK2_CK** 0: Power on 1: Power down
5	RG_DRV_ISINK1_CK_PDN	**Powers down DRV_ISINK1_CK** 0: Power on 1: Power down
4	RG_DRV_ISINK0_CK_PDN	**Powers down DRV_ISINK0_CK** 0: Power on 1: Power down
3	RG_DRV_32K_CK_PDN	**Powers down DRV_32K_CK** 0: Power on 1: Power down
2	RG_G_DRV_2M_CK_PDN	**Powers down G_DRV_2M_CK** 0: Power on 1: Power down
1	RG_G_SMPS_AUD_CK_PDN	**Powers down G_SMPS_AUD_CK** 0: Power on 1: Power down
0	RG_G_SMPS_PD_CK_PDN	**Powers down G_SMPS_PD_CK** 0: Power on 1: Power down

023E **TOP_CKPDN_CON0_SET** **TOP_CKPDN_CON0 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON0_SET	**Sets up TOP_CKPDN_CON0** 1'b0: Does not set 1'b1: Set

0240 **TOP_CKPDN_CON0_CLR** **TOP_CKPDN_CON0 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON0_CLR	**Clears TOP_CKPDN_CON0** 1'b0: Does not clear

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Bit(s)	Name	Description
		1'b1: Clear

0242 **TOP_CKPDN_CON1** **TOP_CKPDN Control Register 1** **04A0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_PWMOC_6M_CK_PDN	RG_AUXADC_CK_PDN	RG_BUCK_1M_CK_PDN	RG_STB_1M_CK_PDN	RG_FQMTR_CK_PDN	RG_RTC_2SEC_OFF_DET_PDN	RG_RTC32K_1V8_1_O_PDN	RG_RTC32K_1V8_0_O_PDN	RG_RTCDET_CK_PDN	RG_RTC_75K_CK_PDN	RG_RTC_MCLK_PDN	RG_RTC_32K_CK_PDN
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	1	0	0	1	0	1	0	0	0	0	0

Bit(s)	Name	Description
11	RG_PWMOC_6M_CK_PDN	**Powers down PWMOC_6M_CK** 0: Power on 1: Power down
10	RG_AUXADC_CK_PDN	**Powers down AUXADC_CK** 0: Power on 1: Power down
9	RG_BUCK_1M_CK_PDN	**Powers down BUCK_1M_CK** 0: Power on 1: Power down
8	RG_STB_1M_CK_PDN	**Powers down STB_1M_CK** 0: Power on 1: Power down
7	RG_FQMTR_CK_PDN	**Powers down FQMTR_CK** 0: Power on 1: Power down
6	RG_RTC_2SEC_OFF_DET_PDN	**Powers down RTC_2SEC_OFF_DET** 0: Power on 1: Power down
5	RG_RTC32K_1V8_1_O_PDN	**Powers down RTC32K_1V8_1_O** 0: Power on 1: Power down
4	RG_RTC32K_1V8_0_O_PDN	**Powers down RTC32K_1V8_0_O** 0: Power on 1: Power down
3	RG_RTCDET_CK_PDN	**Powers down RTCDET_CK** 0: Power on 1: Power down
2	RG_RTC_75K_CK_PDN	**Powers down RTC_75K_CK** 0: Power on 1: Power down
1	RG_RTC_MCLK_PDN	**Powers down RTC_MCLK** 0: Power on 1: Power down

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Bit(s)	Name	Description
0	RG_RTC_32K_CK_PDN	**Powers down RTC_32K_CK** 0: Power on 1: Power down

0244 TOP_CKPDN_CON1_SET TOP_CKPDN_CON1 Register SET 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON1_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON1_SET	**Sets up TOP_CKPDN_CON1** 1'b0: Does not set 1'b1: Set

0246 TOP_CKPDN_CON1_CLR TOP_CKPDN_CON1 Register CLR 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON1_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON1_CLR	**Clears TOP_CKPDN_CON1** 1'b0: Does not clear 1'b1: Clear

0248 TOP_CKPDN_CON2 TOP_CKPDN Control Register 2 167F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_STRUP_LBAT_SEL_CK_PDN	RG_TRIM_75K_CK_PDN	RG_RTC_EOSC32_CK_PDN	RG_RTC_26M_CK_PDN	RG_INTRP_CK_PDN	RG_FQMTR_32K_CK_PDN	RG_ACCDET_CK_PDN		RG_PCHR_32K_CK_PDN	RG_BIFX1_CK_PDN	RG_BIFX4_CK_PDN	RG_BIFX72_CK_PDN	RG_FGADC_DIG_CK_PDN	RG_FGADC_ANA_CK_PDN	RG_SPK_PWM_CK_PDN	RG_SPK_CK_PDN
Type	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	1	0	1	1		0	1	1	1	1	1	1	1

Bit(s)	Name	Description
15	RG_STRUP_LBAT_SEL_CK_PDN	**Powers down STRUP_LBAT_SEL_CK** 0: Power on 1: Power down

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Bit(s)	Name	Description
14	RG_TRIM_75K_CK_PDN	**Powers down TRIM_75K_CK** 0: Power on 1: Power down
13	RG_RTC_EOSC32_CK_PDN	**Powers down RTC_EOSC32_CK** 0: Power on 1: Power down
12	RG_RTC_26M_CK_PDN	**Powers down RTC_26M_CK** 0: Power on 1: Power down
11	RG_INTRP_CK_PDN	**Powers down INTRP_CK** 0: Power on 1: Power down
10	RG_FQMTR_32K_CK_PDN	**Powers down FQMTR_32K_CK** 0: Power on 1: Power down
9	RG_ACCDET_CK_PDN	**Powers down ACCDET_CK** 0: Power on 1: Power down
7	RG_PCHR_32K_CK_PDN	**Powers down PCHR_32K_CK** 0: Power on 1: Power down
6	RG_BIF_X1_CK_PDN	**Powers down BIF_X1_CK** 0: Power on 1: Power down
5	RG_BIF_X4_CK_PDN	**Powers down BIF_X4_CK** 0: Power on 1: Power down
4	RG_BIF_X72_CK_PDN	**Powers down BIF_X72_CK** 0: Power on 1: Power down
3	RG_FGADC_DIG_CK_PDN	**Powers down FGADC_DIG_CK** 0: Power on 1: Power down
2	RG_FGADC_ANA_CK_PDN	**Powers down FGADC_ANA_CK** 0: Power on 1: Power down
1	RG_SPK_PWM_CK_PDN	**Powers down SPK_PWM_CK** 0: Power on 1: Power down
0	RG_SPK_CK_PDN	**Powers down SPK_CK** 0: Power on 1: Power down

024A **TOP_CKPDN_CON2_SET** **TOP_CKPDN_CON2 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON2_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	TOP_CKPDN_CON2_SET	**Sets up TOP_CKPDN_CON2** 1'b0: Does not set 1'b1: Set

024C **TOP_CKPDN_CON2_CLR** **TOP_CKPDN_CON2 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON2_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON2_CLR	**Clears TOP_CKPDN_CON2** 1'b0: Does not clear 1'b1: Clear

024E **TOP_CKPDN_CON3** **TOP_CKPDN control register 3** **05E0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_EOSC_CALI_TEST_CK_PDN	RG_BUCK_ANA_CK_PDN	RG_BUCK_32K_CK_PDN	RG_PCHR_TEST_CK_PDN	RG_FGADC_FT_CK_PDN	RG_BGR_TEST_CK_PDN	RG_SPI_CK_PDN	RG_SMPS_CK_DIV_PDN	RG_EFUSE_CK_PDN	RG_STRUP_32K_CK_PDN	RG_STRUP_75K_CK_PDN
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset						1	0	1	1	1	1	0	0	0	0	0

Bit(s)	Name	Description
10	RG_EOSC_CALI_TEST_CK_PDN	**Powers down EOSC_CALI_TEST_CK** 0: Power on 1: Power down
9	RG_BUCK_ANA_CK_PDN	**Powers down BUCK_ANA_CK** 0: Power on 1: Power down
8	RG_BUCK_32K_CK_PDN	**Powers down BUCK_32K_CK** 0: Power on 1: Power down
7	RG_PCHR_TEST_CK_PDN	**Powers down PCHR_TEST_CK** 0: Power on 1: Power down
6	RG_FGADC_FT_CK_PDN	**Powers down FGADC_FT_CK** 0: Power on 1: Power down
5	RG_BGR_TEST_CK_PDN	**Powers down BGR_TEST_CK** 0: Power on

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Bit(s)	Name	Description
		1: Power down
4	RG_SPI_CK_PDN	**Powers down SPI_CK** 0: Power on 1: Power down
3	RG_SMPS_CK_DIV_PDN	**Powers down SMPS_CK_DIV** 0: Power on 1: Power down
2	RG_EFUSE_CK_PDN	**Powers down EFUSE_CK** 0: Power on 1: Power down
1	RG_STRUP_32K_CK_PDN	**Powers down STRUP_32K_CK** 0: Power on 1: Power down
0	RG_STRUP_75K_CK_PDN	**Powers down STRUP_75K_CK** 0: Power on 1: Power down

0250 **TOP_CKPDN_CON3_SET** **TOP_CKPDN_CON3 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON3_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON3_SET	**Sets up TOP_CKPDN_CON3** 1'b0: Does not set 1'b1: Set

0252 **TOP_CKPDN_CON3_CLR** **TOP_CKPDN_CON3 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON3_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON3_CLR	**Clears TOP_CKPDN_CON3** 1'b0: Does not clear 1'b1: Clear

0254 **TOP_CKPDN_CON4** **TOP_CKPDN control register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_	RG_	RG_	RG_	RG_	RG_	RG_

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											BUCK_VPROC_18M_CK_PDN	BUCK_VCORE1_18M_CK_PDN	BUCK_VSYS22_18M_CK_PDN	BUCK_VLTE_18M_CK_PDN	BUCK_VPA_18M_CK_PDN	BUCK_VSRAM_18M_CK_PDN	BUCK_18M_CK_PDN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	RG_BUCK_VPROC_18M_CK_PDN	**Powers down BUCK_VPROC_18M_CK** 0: Power on 1: Power down
5	RG_BUCK_VCORE1_18M_CK_PDN	**Powers down BUCK_VCORE1_18M_CK** 0: Power on 1: Power down
4	RG_BUCK_VSYS22_18M_CK_PDN	**Powers down BUCK_VSYS22_18M_CK** 0: Power on 1: Power down
3	RG_BUCK_VLTE_18M_CK_PDN	**Powers down BUCK_VLTE_18M_CK** 0: Power on 1: Power down
2	RG_BUCK_VPA_18M_CK_PDN	**Powers down BUCK_VPA_18M_CK** 0: Power on 1: Power down
1	RG_BUCK_VSRAM_18M_CK_PDN	**Powers down BUCK_VSRAM_18M_CK** 0: Power on 1: Power down
0	RG_BUCK_18M_CK_PDN	**Powers down BUCK_18M_CK** 0: Power on 1: Power down

0256 TOP_CKPDN_CON4_SET TOP_CKPDN_CON4 Register SET 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON4_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON4_SET	**Sets up TOP_CKPDN_CON4** 1'b0: Does not set 1'b1: Set

0258 TOP_CKPDN_CON4_CLR TOP_CKPDN_CON4 Register CLR 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKPDN_CON4_CLR															
Type	W1															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKPDN_CON4_CLR	**Clears TOP_CKPDN_CON4** 1'b0: Does not clear 1'b1: Clear

025A TOP_CKSEL_CON0 TOP_CKSEL Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SRCLKEN_SRC_SEL		RG_OSC_SEL_HW_SRC_SEL			RG_AUXADC_CK_CKSEL	RG_75K_32K_SEL	RG_FQMTR_CK_CKSEL			RG_DRV_ISINK3_CK_CKSEL	RG_DRV_ISINK2_CK_CKSEL	RG_DRV_ISINK1_CK_CKSEL	RG_DRV_ISINK0_CK_CKSEL	RG_AUD_CK_CKSEL	RG_AUDIF_CK_CKSEL
Type	RW		RW			RW	RW	RW			RW	RW	RW	RW	RW	RW
Reset	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:14	RG_SRCLKEN_SRC_SEL	**Selects srclken source** 2'b00: From srclken0 2'b01: From srclken1 2'b10: From srclken0 and srclken1 2'b11: Reserved
13:12	RG_OSC_SEL_HW_SRC_SEL	**Selects OSC_SEL source under hardware control** 2'b00: From buck controller 2'b01: From srclken 2'b10: Reserved 2'b11: Reserved
10	RG_AUXADC_CK_CKSEL	**Selects AUXADC_CK clock** 1'b0: R_SMPS_CK/n 1'b1: R_AUD26_CK/n
9	RG_75K_32K_SEL	**Selects RTC_32K1V8_CK clock** 1'b0: R_PMU75K_CK/2 1'b1: R_RTC32K_CK
8:6	RG_FQMTR_CK_CKSEL	**Selects FQMTR_CK clock** 3'b000: R_AUD_26M_CK 3'b001: R_XOSC32_CK_DETECTION 3'b010: R_EOSC32_CK 3'b011: R_RTC32K_CK 3'b100: R_SMPS_CK 3'b101: R_RTC_TICK_SEC 3'b11x: R_PMU75K_CK
5	RG_DRV_ISINK3_CK_CKSEL	**Selects DRV_ISINK3_CK clock** 1'b0: R_RTC32K_CK 1'b1: G_DRV_2M_CK
4	RG_DRV_ISINK2_CK_CKSEL	**Selects DRV_ISINK2_CK clock** 1'b0: R_RTC32K_CK 1'b1: G_DRV_2M_CK
3	RG_DRV_ISINK1_CK_CKSEL	**Selects DRV_ISINK1_CK clock** 1'b0: R_RTC32K_CK

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Bit(s)	Name	Description
		1'b1: G_DRV_2M_CK
2	RG_DRV_ISINK0_CK_CKSEL	**Selects DRV_ISINK0_CK clock** 1'b0: R_RTC32K_CK 1'b1: G_DRV_2M_CK
1	RG_AUD_CK_CKSEL	**Selects AUD_CK clock** 1'b0: R_AUD_26M_CK 1'b1: R_PAD_AUDIF_CK
0	RG_AUDIF_CK_CKSEL	**Selects AUDIF_CK clock** 1'b0: R_PAD_AUDIF_CK 1'b1: R_AUD_26M_CK

025C **TOP_CKSEL_CON0_SET** **TOP_CKSEL_CON0 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKSEL_CON_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKSEL_CON_SET	**Sets up TOP_CKSEL_CON0** 1'b0: Does not set 1'b1: Set

025E **TOP_CKSEL_CON0_CLR** **TOP_CKSEL_CON0 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKSEL_CON_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKSEL_CON_CLR	**Clears TOP_CKSEL_CON0** 1'b0: Does not clear 1'b1: Clear

0260 **TOP_CKSEL_CON1** **TOP_CKSEL control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_FGADC_ANA_CK_CKSEL	RG_PCHR_TEST_CK_CKSEL	RG_BGR_TEST_CK_CKSEL	RG_STRUP_75K_CK_CKSEL	
Type												RW	RW	RW	RW	

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Reset												0	0	0	0	0

Bit(s)	Name	Description
4	RG_FGADC_ANA_CK_CKSEL	**Selects FGADC_ANA_CK clock** 1'b0: R_RTC32K_CK 1'b1: FGADC_FT_CK_DIV8
3	RG_PCHR_TEST_CK_CKSEL	**Selects PCHR_TEST_CK clock** 1'b0: R_AUD_26M_CK 1'b1: R_SMPS_CK
2	RG_BGR_TEST_CK_CKSEL	**Selects BGR_TEST_CK clock** 1'b0: R_AUD_26M_CK 1'b1: R_SMPS_CK
1:0	RG_STRUP_75K_CK_CKSEL	**Selects STRUP_75K_CK clock** 2'b00: R_PMU75K_CK 2'b01: R_AUD_26M_CK 2'b1x: R_SMPS_CK

0262 **TOP_CKSEL_CON1_SET** **TOP_CKSEL_CON1 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKSEL_CON1_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKSEL_CON1_SET	**Sets up TOP_CKSEL_CON1** 1'b0: Does not set 1'b1: Set

0264 **TOP_CKSEL_CON1_CLR** **TOP_CKSEL_CON1 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKSEL_CON1_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKSEL_CON1_CLR	**Clears TOP_CKSEL_CON1** 1'b0: Does not clear 1'b1: Clear

0266 **TOP_CKSEL_CON2** **TOP_CKSEL Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							TOP		RG_	RG_		RG_	RG_	RG_		RG_

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							_CKSEL_CON2_RSV		**VCORE2_OSC_SEL_MODE**	**BUCK_OSC_SEL_MODE**		**SRCVOLTEN_MODE**	**VCORE2_OSC_SEL_SW**	**BUCK_OSC_SEL_SW**		**SRCVOLTEN_SW**
Type							RW		RW	RW		RW	RW	RW		RW
Reset							0		0	0		0	0	0		0

Bit(s)	Name	Description
9	TOP_CKSEL_CON2_RSV	
7	RG_VCORE2_OSC_SEL_MODE	**VCORE2_OSC_SEL mode** 1'b0: HW mode 1'b1: SW mode
6	RG_BUCK_OSC_SEL_MODE	**BUCK_OSC_SEL mode** 1'b0: HW mode 1'b1: SW mode
4	RG_SRCVOLTEN_MODE	**SRCVOLTEN mode** 1'b0: HW mode 1'b1: SW mode
3	RG_VCORE2_OSC_SEL_SW	**VCORE2_OSC_SEL SW mode value**
2	RG_BUCK_OSC_SEL_SW	**BUCK_OSC_SEL SW mode value**
0	RG_SRCVOLTEN_SW	**SRCVOLTEN SW mode value**

0268 TOP_CKSEL_CON2_SET TOP_CKSEL_CON2 Register SET 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKSEL_CON2_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKSEL_CON2_SET	**Sets up TOP_CKSEL_CON2** 1'b0: Does not set 1'b1: Set

026A TOP_CKSEL_CON2_CLR TOP_CKSEL_CON2 Register CLR 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKSEL_CON2_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15:0	TOP_CKSEL_CON2_CLR	**Clears TOP_CKSEL_CON2** 1'b0: Does not clear 1'b1: Clear

026C TOP_CKDIVSEL_CON0 TOP_CKDIVSEL Control Register 0 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SPK_PWM_CK_DIVSEL		RG_SPK_CK_DIVSEL				RG_REG_CK_DIVSEL			RG_BIF_X4_CK_DIVSEL					RG_STRUP_LBAT_SEL_CK_DIVSEL	
Type	RW		RW				RW			RW					RW	
Reset	0	0	0	0			0	0		0	0	0			0	1

Bit(s)	Name	Description
15:14	RG_SPK_PWM_CK_DIVSEL	**Selects SPK_PWM_CK divider** 2'b00: DIV1 2'b01: DIV16 2'b10: DIV32 2'b11: DIV64
13:12	RG_SPK_CK_DIVSEL	**Selects SPK_CK divider** 2'b00: DIV1 2'b01: DIV2 2'b10: DIV4 2'b11: DIV8
9:8	RG_REG_CK_DIVSEL	**Selects REG_CK divider** 2'b00: DIV1 2'b01: DIV2 2'b10: DIV4 2'b11: DIV8
6:4	RG_BIF_X4_CK_DIVSEL	**Selects BIF_X4_CK divider** 3'b000: DIV1 3'b001: DIV2 3'b010: DIV4 3'b011: DIV8 3'b1xx: DIV16
1:0	RG_STRUP_LBAT_SEL_CK_DIVSEL	**Selects STRUP_LBAT_SEL_CK divider** 2'b00: DIV18 2'b01: DIV9 2'b10: DIV4 2'b11: DIV2

026E TOP_CKDIVSEL_CON0_SET TOP_CKDIVSEL_CON0 Register SET 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKDIVSEL_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	TOP_CKDIVSEL_CON0_SET	**Sets up TOP_CKDIVSEL_CON0** 1'b0: Does not set 1'b1: Set

0270	TOP_CKDIVSEL_CON0_CLR	TOP_CKDIVSEL_CON0 Register CLR	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKDIVSEL_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKDIVSEL_CON0_CLR	**Clears TOP_CKDIVSEL_CON0** 1'b0: Does not clear 1'b1: Clear

0272	TOP_CKDIVSEL_CON1	TOP_CKDIVSEL Control Register 1	0015

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_BUCK_18M_CK_DIVSEL	RG_AUXADC_26M_CK_DIVSEL		RG_AUXADC_SMPS_CK_DIVSEL	
Type												RW	RW		RW	
Reset												1	0	1	0	1

Bit(s)	Name	Description
4	RG_BUCK_18M_CK_DIVSEL	**Selects BUCK_18M_CK divider** 1'b0: DIV1 1'b1: DIV2
3:2	RG_AUXADC_26M_CK_DIVSEL	**Selects AUXADC_26M_CK divider** 2'b00: DIV26 2'b01: DIV13 2'b1x: DIV8
1:0	RG_AUXADC_SMPS_CK_DIVSEL	**Selets AUXADC_SMPS_CK divider** 2'b00: DIV18 2'b01: DIV9 2'b10: DIV6 2'b11: DIV4

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0274 TOP_CKDIVSEL_CON1_SET — TOP_CKDIVSEL_CON1 Register SET — 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKDIVSEL_CON1_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKDIVSEL_CON1_SET	**Sets up TOP_CKDIVSEL_CON1** 1'b0: Does not set 1'b1: Set

0276 TOP_CKDIVSEL_CON1_CLR — TOP_CKDIVSEL_CON1 Register CLR — 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKDIVSEL_CON1_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKDIVSEL_CON1_CLR	**Clears TOP_CKDIVSEL_CON1** 1'b0: Does not clear 1'b1: Clear

0278 TOP_CKHWEN_CON0 — TOP_CKHWEN control register 0 — 30FF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUXADC_CK_CKSEL_HWEN	RG_AUXADC_26M_CK_PDN_HWEN			RG_RTC_26M_CK_PDN_HWEN	RG_EFUSE_CK_PDN_HWEN	RG_BUCK_1M_CK_PDN_HWEN	RG_AUXADC_SMPS_CK_PDN_HWEN	RG_AUXADC_CK_PDN_HWEN	RG_G_DRV_2M_CK_PDN_HWEN	RG_G_SMPS_AUD_CK_PDN_HWEN	RG_G_SMPS_PD_CK_PDN_HWEN
Type					RW	RW			RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0			1	1	1	1	1	1	1	1

Bit(s)	Name	Description
11	RG_AUXADC_CK_CKSEL_HWEN	**AUXADC_CK clock selection control** 0: SW mode 1: HW mode
10	RG_AUXADC_26M_CK_PDN_HWEN	**AUXADC_26m_CK clock selection control** 0: SW mode 1: HW mode
7	RG_RTC_26M_CK	**RTC_26M_CK power down control**

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Bit(s)	Name	Description
	_PDN_HWEN	0: SW mode 1: HW mode
6	RG_EFUSE_CK_PDN_HWEN	**EFUSE_CK power down control** 0: SW mode 1: HW mode
5	RG_BUCK_1M_CK_PDN_HWEN	**BUCK_1M_CK power down control** 0: SW mode 1: HW mode
4	RG_AUXADC_SMPS_CK_PDN_HWEN	**AUXADC_SMPS_CK power down control** 0: SW mode 1: HW mode
3	RG_AUXADC_CK_PDN_HWEN	**AUXADC_CK power down control** 0: SW mode 1: HW mode
2	RG_G_DRV_2M_CK_PDN_HWEN	**G_DRV_2M_CK power down control** 0: SW mode 1: HW mode
1	RG_G_SMPS_AUD_CK_PDN_HWEN	**G_SMPS_AUD_CK power down control** 0: SW mode 1: HW mode
0	RG_G_SMPS_PD_CK_PDN_HWEN	**G_SMPS_PD_CK power down control** 0: SW mode 1: HW mode

027A **TOP_CKHWEN_CON0_SET** **TOP_CKHWEN_CON0 Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKHWEN_CON0_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKHWEN_CON0_SET	**Sets up TOP_CKHWEN_CON0** 1'b0: Does not set 1'b1: Set

027C **TOP_CKHWEN_CON0_CLR** **TOP_CKHWEN_CON0 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKHWEN_CON0_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKHWEN_CO	**Clears TOP_CKHWEN_CON0**

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Bit(s)	Name	Description
	No_CLR	1'b0: Does not clear 1'b1: Clear

027E TOP_CKHWEN_CON1 TOP_CKHWEN control register 1 303F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_BUCK_VPROC_18M_CK_PDN_HWEN	RG_BUCK_VCORE1_18M_CK_PDN_HWEN	RG_BUCK_VSYS22_18M_CK_PDN_HWEN	RG_BUCK_VLTE_18M_CK_PDN_HWEN	RG_BUCK_VPA_18M_CK_PDN_HWEN	RG_BUCK_VSRAM_18M_CK_PDN_HWEN
Type											RW	RW	RW	RW	RW	RW
Reset											1	1	1	1	1	1

Bit(s)	Name	Description
5	RG_BUCK_VPROC_18M_CK_PDN_HWEN	**BUCK_VPROC_18M_CK power down control** 0: SW mode 1: HW mode
4	RG_BUCK_VCORE1_18M_CK_PDN_HWEN	**BUCK_VCORE1_18M_CK power down control** 0: SW mode 1: HW mode
3	RG_BUCK_VSYS22_18M_CK_PDN_HWEN	**BUCK_VSYS22_18M_CK power down control** 0: SW mode 1: HW mode
2	RG_BUCK_VLTE_18M_CK_PDN_HWEN	**BUCK_VLTE_18M_CK power down control** 0: SW mode 1: HW mode
1	RG_BUCK_VPA_18M_CK_PDN_HWEN	**BUCK_VPA_18M_CK power down control** 0: SW mode 1: HW mode
0	RG_BUCK_VSRAM_18M_CK_PDN_HWEN	**BUCK_VSRAM_18M_CK power down control** 0: SW mode 1: HW mode

0280 TOP_CKHWEN_CON1_SET TOP_CKHWEN_CON1 Register SET 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKHWEN_CON1_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKHWEN_CO	**Sets up TOP_CKHWEN_CON1**

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Bit(s)	Name	Description
	N1_SET	1'b0: Does not set 1'b1: Set

0282 **TOP_CKHWEN_CON1_CLR** **TOP_CKHWEN_CON1 Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CKHWEN_CON1_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CKHWEN_CON1_CLR	**Clears TOP_CKHWEN_CON1** 1'b0: Does not clear 1'b1: Clear

028A **TOP_CLKSQ** **TOP_CLKSQ Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CLKSQ_EN_VA28						RG_CLKSQ_EN_AUX_MD_MODE	RG_CLKSQ_EN_AUX_AP_MODE				RG_CLKSQ_EN_AUX_GPS	RG_CLKSQ_EN_AUX_MD	RG_CLKSQ_EN_AUX_AP	RG_CLKSQ_EN_FQR	RG_CLKSQ_EN_AUD
Type	RO						RW	RW				RW	RW	RW	RW	RW
Reset	0						0	0				0	0	0	0	0

Bit(s)	Name	Description
15	DA_CLKSQ_EN_VA28	**Status of CLKSQ** 0: Disable 1: Enable
9	RG_CLKSQ_EN_AUX_MD_MODE	**Selects CLKSQ_EN_AUX_MD mode** 0: SW mode 1: HW mode: SRCLKEN_IN0
8	RG_CLKSQ_EN_AUX_AP_MODE	**Selects CLKSQ_EN_AUX_AP mode** 0: SW mode 1: HW mode: SRCLKEN_IN0
4	RG_CLKSQ_EN_AUX_GPS	**Enables CLKSQ for GPS** 0: Disable clock 1: Enable clock
3	RG_CLKSQ_EN_AUX_MD	**Enables CLKSQ for MD (SW mode)** 0: Disable clock 1: Enable clock
2	RG_CLKSQ_EN_AUX_AP	**Enables CLKSQ for AP (SW mode)** 0: Disable clock 1: Enable clock

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Bit(s)	Name	Description
1	RG_CLKSQ_EN_FQR	**Enables CLKSQ for FQMTR** 0: Disable clock 1: Enable clock
0	RG_CLKSQ_EN_AUD	**Enables CLKSQ for AUDIO** 0: Disable clock 1: Enable clock

028C **TOP_CLKSQ_SET** **TOP_CLKSQ Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CLKSQ_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CLKSQ_SET	**Sets up TOP_CLKSQ** 1'b0: Does not set 1'b1: Set

028E **TOP_CLKSQ_CLR** **TOP_CLKSQ Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CLKSQ_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CLKSQ_CLR	**Clears TOP_CLKSQ** 1'b0: Does not clear 1'b1: Clear

0290 **TOP_CLKSQ_RTC** **TOP_CLKSQ_RTC Register** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_CLKSQ_EN_VDIG18														RG_CLKSQ_RTC_EN_HW_MODE	RG_CLKSQ_RTC_EN
Type	RO														RW	RW
Reset	0														1	0

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Bit(s)	Name	Description
15	DA_CLKSQ_EN_VDIG18	**Status of CLKSQ_RTC** 0: Disable 1: Enable
1	RG_CLKSQ_RTC_EN_HW_MODE	**CLKSQ_RTC HW mode** If enable, CLKSQ_RTC will be from HW control; if disable, CLKSQ_RTC will be from RG_CLKSQ_RTC_EN. 0: SW mode 1: HW mode
0	RG_CLKSQ_RTC_EN	**Enables CLKSQ_RTC** 0: Disable clock 1: Enable clock

0292 **TOP_CLKSQ_RTC_SET** **TOP_CLKSQ_RTC Register SET** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CLKSQ_RTC_SET															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CLKSQ_RTC_SET	**Sets up TOP_CLKSQ_RTC** 1'b0: Does not set 1'b1: Set

0294 **TOP_CLKSQ_RTC_CLR** **TOP_CLKSQ_RTC Register CLR** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_CLKSQ_RTC_CLR															
Type	W1															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TOP_CLKSQ_RTC_CLR	**Clears TOP_CLKSQ_RTC** 1'b0: Does not clear 1'b1: Clear

0296 **TOP_CLK_TRIM** **TOP_CLK_TRIM Register** **0C6C**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_OSC_75K_TRIM												
Type				RO												
Reset				0	1	1	0	0								

Bit(s)	Name	Description

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Bit(s)	Name	Description
12:8	RG_OSC_75K_TRIM	**75kHz OSC trimming bit**

0418	BUCK_ALL_CON18	Buck All Control Register 18	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												VPA_OC_FLAG_CLR	VSYS22_OC_FLAG_CLR	VCORE1_OC_FLAG_CLR	VLTE_OC_FLAG_CLR	VPROC_OC_FLAG_CLR
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	VPA_OC_FLAG_CLR	**0: Keep OC status** 1: Clear OC status
3	VSYS22_OC_FLAG_CLR	**0: Keep OC status** 1: Clear OC status
2	VCORE1_OC_FLAG_CLR	**0: Keep OC status** 1: Clear OC status
1	VLTE_OC_FLAG_CLR	**0: Keep OC status** 1: Clear OC status
0	VPROC_OC_FLAG_CLR	**0: Keep OC status** 1: Clear OC status

041A	BUCK_ALL_CON19	Buck All Control Register 19	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												VPA_OC_FLAG_CLR_SEL	VSYS22_OC_FLAG_CLR_SEL	VCORE1_OC_FLAG_CLR_SEL	VLTE_OC_FLAG_CLR_SEL	VPROC_OC_FLAG_CLR_SEL
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	VPA_OC_FLAG_CLR_SEL	0: HW clear OC status 1: SW clear OC status
3	VSYS22_OC_FLAG_CLR_SEL	0: HW clear OC status 1: SW clear OC status
2	VCORE1_OC_FLAG_CLR_SEL	0: HW clear OC status 1: SW clear OC status

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Bit(s)	Name	Description
1	VLTE_OC_FLAG_CLR_SEL	0: HW clear OC status 1: SW clear OC status
0	VPROC_OC_FLAG_CLR_SEL	0: HW clear OC status 1: SW clear OC status

0420 **BUCK_ALL_CON22** **Buck All Control Register 22** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												VPA_EN_OC_SDN_SEL	VSYS22_EN_OC_SDN_SEL	VCORE1_EN_OC_SDN_SEL	VLTE_EN_OC_SDN_SEL	VPROC_EN_OC_SDN_SEL
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	VPA_EN_OC_SDN_SEL	0: Enable OC shut-down 1: Disable OC shut-down
3	VSYS22_EN_OC_SDN_SEL	0: Enable OC shut-down 1: Disable OC shut-down
2	VCORE1_EN_OC_SDN_SEL	0: Enable OC shut-down 1: Disable OC shut-down
1	VLTE_EN_OC_SDN_SEL	0: Enable OC shut-down 1: Disable OC shut-down
0	VPROC_EN_OC_SDN_SEL	0: Enable OC shut-down 1: Disable OC shut-down

042E **SMPS_TOP_ANA_CON0** **SMPS_TOP Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VPROC_TRIMH					RG_SMPS_TESTMODE_B								
Type			RW					RW								
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:9	RG_VPROC_TRIMH	**Fine-tunes R2R DAC reference** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV

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Bit(s)	Name	Description
		10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV
8:0	RG_SMPS_TESTMODE_B	**Test mode enable bit** Default 0: Disable testmode (Default) NORMAL: 8'b00000000 [0]: 0: VBUF GOOD 1: VBUF not good [3:1]: N/A [4] CSM measure from LDO bist 0: No value 1: CSM from LDO bist [7:5]: CSM measurement selection 000: N/A 001: N/A 010: VCORE1 011: VLTE 100: N/A 101: VPROC 110: VSYS22 111: N/A [8]: Pass CSM signal to KP_LED or AUXADC 0: Disable 1: Enable

0430 **SMPS_TOP_ANA_CON1** **SMPS_TOP control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_VCORE1_TRIML					RG_VCORE1_TRIMH					RG_VPROC_TRIML				
Type		RW					RW					RW				
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:10	RG_VCORE1_TRIML	**Fine-tunes R2R DAC reference** 11111: Vo offset=+6.25mV

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Bit(s)	Name	Description
		11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV
9:5	RG_VCORE1_TRIMH	**Fine-tunes R2R DAC reference** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV

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Bit(s)	Name	Description
		01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV
4:0	RG_VPROC_TRIML	**Fine-tunes R2R DAC reference** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV

0432	**SMPS_TOP_ANA_CON2**	**SMPS_TOP control register 2**	**0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VSYS22_TRIMH				RG_VLTE_TRIML					RG_VLTE_TRIMH				
Type			RW				RW					RW				
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:10	RG_VSYS22_TRIMH	**Fine-tunes R2R DAC reference** 1111: Vo offset=+6.25mV 1110: Vo offset=+12.5mV 1101: Vo offset=+18.75mV 1100: Vo offset=+25mV 1011: Vo offset=+31.25mV 1010: Vo offset=+37.5mV 1001: Vo offset=+43.75mV 0000: Vo offset=0mV (default) 0001: Vo offset=-6.25mV 0010: Vo offset=-12.5mV

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Bit(s)	Name	Description
		0011: Vo offset=-18.75mV 0100: Vo offset=-25mV 0101: Vo offset=-31.25mV 0110: Vo offset=-37.5mV 0111: Vo offset=-43.75mV 1000: Vo offset=-50mV
9:5	RG_VLTE_TRIML	**Fine-tunes R2R DAC reference** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV
4:0	RG_VLTE_TRIMH	**Fine-tunes R2R DAC reference** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV

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Bit(s)	Name	Description
		00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV

0434 **SMPS_TOP_ANA_CON3** **SMPS_TOP control register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VPA_TRIML					RG_VPA_TRIMH					RG_VSYS22_TRIML			
Type			RW					RW					RW			
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:9	RG_VPA_TRIML	**Fine-tunes R2R DAC reference** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV
8:4	RG_VPA_TRIMH	**Fine-tunes R2R DAC reference** 11111: Vo offset=+6.25mV

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Bit(s)	Name	Description
		11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV
3:0	RG_VSYS22_TRIML	**Fine-tunes R2R DAC reference** 1111: Vo offset=+6.25mV 1110: Vo offset=+12.5mV 1101: Vo offset=+18.75mV 1100: Vo offset=+25mV 1011: Vo offset=+31.25mV 1010: Vo offset=+37.5mV 1001: Vo offset=+43.75mV 0000: Vo offset=0mV (default) 0001: Vo offset=-6.25mV 0010: Vo offset=-12.5mV 0011: Vo offset=-18.75mV 0100: Vo offset=-25mV 0101: Vo offset=-31.25mV 0110: Vo offset=-37.5mV 0111: Vo offset=-43.75mV 1000: Vo offset=-50mV

0436 SMPS_TOP_ANA_CON4 SMPS_TOP control register 4 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_VSRAM_TRIML					RG_VSRAM_TRIMH				
Type							RW					RW				
Reset							0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
9:5	RG_VSRAM_TRIML	**Fine-tunes R2R DAC reference** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV
4:0	RG_VSRAM_TRIMH	**Fine-tunes R2R DAC reference** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV 11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV

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Bit(s)	Name	Description
		01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV

0438 **SMPS_TOP_ANA_CON5** **SMPS_TOP Control Register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VPA_BURSTH		RG_VLTE_VSLEEP			RG_VCORE1_VSLEEP			RG_VPROC_VSLEEP			RG_VPA_TRIM_REF				
Type	RW		RW			RW			RW			RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:14	RG_VPA_BURSTH	**PWM/BURST threshold** 00: VH=0.50V (default) 01: VH=0.45V 10: VH=0.55V 11: VH=0.60V
13:11	RG_VLTE_VSLEEP	**Selects sleep mode voltage** 000: VSLEEP 001: VSLEEP - 12.5mV 010: VSLEEP - 12.5mV*2 011: VSLEEP - 12.5mV*3 100: VSLEEP + 12.5mV*4 101: VSLEEP + 12.5mV*3 110: VSLEEP + 12.5mV*2 111: VSLEEP + 12.5mV
10:8	RG_VCORE1_VSLEEP	**Selects sleep mode voltage** 000: VSLEEP 001: VSLEEP - 12.5mV 010: VSLEEP - 12.5mV*2 011: VSLEEP - 12.5mV*3 100: VSLEEP + 12.5mV*4 101: VSLEEP + 12.5mV*3 110: VSLEEP + 12.5mV*2 111: VSLEEP + 12.5mV
7:5	RG_VPROC_VSLEEP	**Selects sleep mode voltage** 000: VSLEEP 001: VSLEEP - 12.5mV 010: VSLEEP - 12.5mV*2 011: VSLEEP - 12.5mV*3 100: VSLEEP + 12.5mV*4 101: VSLEEP + 12.5mV*3 110: VSLEEP + 12.5mV*2 111: VSLEEP + 12.5mV
4:0	RG_VPA_TRIM_REF	**Fine-tunes R2R DAC reference** 11111: Vo offset=+6.25mV 11110: Vo offset=+12.5mV 11101: Vo offset=+18.75mV 11100: Vo offset=+25mV 11011: Vo offset=+31.25mV

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Bit(s)	Name	Description
		11010: Vo offset=+37.5mV 11001: Vo offset=+43.75mV 11000: Vo offset=+50mV 10111: Vo offset=+56.25mV 10110: Vo offset=+62.5mV 10101: Vo offset=+68.75mV 10100: Vo offset=+75mV 10011: Vo offset=+81.25mV 10010: Vo offset=+87.5mV 10001: Vo offset=+93.75mV 00000: Vo offset=0mV (default) 00001: Vo offset=-6.25mV 00010: Vo offset=-12.5mV 00011: Vo offset=-18.75mV 00100: Vo offset=-25mV 00101: Vo offset=-31.25mV 00110: Vo offset=-37.5mV 00111: Vo offset=-43.75mV 01000: Vo offset=-50mV 01001: Vo offset=-56.25mV 01010: Vo offset=-62.5mV 01011: Vo offset=-68.75mV 01100: Vo offset=-75mV 01101: Vo offset=-81.25mV 01110: Vo offset=-87.5mV 01111: Vo offset=-93.75mV 10000: Vo offset=-100mV

043A **SMPS_TOP_ANA_CON6** **SMPS_TOP Control Register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_DMY100MA_EN**											**RG_VSRAM_DVFS1_VSLEEP**			**RG_VPA_BURSTL**	
Type	RW											RW			RW	
Reset	0											0	0	0	0	0

Bit(s)	Name	Description
15	RG_DMY100MA_EN	**Selects sleep mode voltage** 0: DMY load off 1: DMY load on
4:2	RG_VSRAM_DVFS1_VSLEEP	**Selects sleep mode voltage** 000: VSLEEP 001: VSLEEP - 12.5mV 010: VSLEEP - 12.5mV*2 011: VSLEEP - 12.5mV*3 100: VSLEEP + 12.5mV*4 101: VSLEEP + 12.5mV*3 110: VSLEEP + 12.5mV*2 111: VSLEEP + 12.5mV
1:0	RG_VPA_BURSTL	**PWM/BURST threshold** 00: VH=0.35V (default) 01: VH=0.30V 10: VH=0.40V

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Bit(s)	Name	Description
		11: VH=0.45V

043C **SMPS_TOP_ANA_CON7** **SMPS_TOP Control Register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_DMY100MA_SEL	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	RG_DMY100MA_SEL	**PWM/BURST threshold** 00: typ Iload (default) 01: 10/8 10: 6/8 11: 4/8

0440 **VCORE_ANA_CON0** **VCORE_ANA Control Register 0** **32A2**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VCORE1_CSL				RG_VCORE1_CSR			RG_VCORE1_RZSEL			RG_VCORE1_1P35UP_SEL_EN	RG_VCORE1_VRF18_SSTART_EN	RG_VCORE1_MIN_OFF	
Type			RW				RW			RW			RW	RW	RW	
Reset			1	1	0	0	1	0	1	0	1	0	0	0	1	0

Bit(s)	Name	Description
13:10	RG_VCORE1_CSL	**Adjusts over current limit** 4'b0000: 6.4A 4'b1000: 5.8A 4'b1100: 5.2A 4'b1110: 4.6A 4'b1110: 4.0A
9:7	RG_VCORE1_CSR	**Adjusts current sense ratio** 3'b000: 18K (800mV) 3'b001: 15.75K (700mV) 3'b010: 13.5K (600mV) 3'b011: 11.25K (500mV) 3'b100: 9K (400mV) 3'b101: 6.75K (300mV) 3'b110: 4.5K (200mV) 3'b111: 2.25K (100mV)
6:4	RG_VCORE1_RZSEL	**Adjusts compensation R** 3'b000: 300 kohm 3'b001: 500 kohm 3'b010: 600 kohm

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Bit(s)	Name	Description
		3'b011: 700 kohm 3'b100: 800 kohm 3'b101: 900 kohm 3'b110: 1000 kohm 3'b111: 1200 kohm
3	RG_VCORE1_1P35UP_SEL_EN	**Selects RDIV** 1'b0: vo<1.35v 1'b1: vo>=1.35v
2	RG_VCORE1_VRF18_SSTART_EN	**Not used**
1:0	RG_VCORE1_MIN_OFF	**Not used**

0442 **VCORE_ANA_CON1** **VCORE_ANA Control Register 1** **101A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VCORE1_NDIS_EN	RG_VCORE1_MODESET	RG_VCORE1_ZXOS_TRIM						RG_VCORE1_ZX_OS		RG_VCORE1_SLP		
Type				RW	RW	RW						RW		RW		
Reset				1	0	0	0	0	0	0	0	1	1	0	1	0

Bit(s)	Name	Description
12	RG_VCORE1_NDIS_EN	**Enables power down NMOS** 1'b1: Enable (default) 1'b0: Disable
11	RG_VCORE1_MODESET	**1'b1: Force PWM mode** 1'b0: Auto mode
10:5	RG_VCORE1_ZXOS_TRIM	**1LSB=175mA** LX zero-crossing offset trimming 6'b000001: +1LSB 6'b000010: +2LSB 6'b000100: +4LSB 6'b001000: -1LSB 6'b010000: -2LSB 6'b100000: -4LSB
4:3	RG_VCORE1_ZX_OS	**nlim offset adjustment combined with RG_VCORE1_RSV[7:6]** RG_VCORE1_RSV[7:6]+RG_VCORE1_ZX_OS[1:0] 1LSB = 175mA 1110: -1LSB 1101: -2LSB 1011: -4LSB 0111: +8LSB
2:0	RG_VCORE1_SLP	**Adjusts slope compensation** 3'b000: 1uA 3'b001: 1.5uA 3'b010: 2uA 3'b011: 2.5uA 3'b100: 3uA 3'b101: 3.5uA

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Bit(s)	Name	Description
		3'b110: 4uA 3'b111: 4.5uA

0444 **VCORE_ANA_CON2** **VCORE_ANA Control Register 2** **0820**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCORE1_CSM_P						RG_VCORE1_CSM_N					
Type					RW						RW					
Reset					1	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
11:6	RG_VCORE1_CSM_P	**Adjusts current measurement** [5]: IMAX=1.5V or 1V 1b'0: 1.5V 1b'1: 1V [4]: Enable test mode 6`bXX0000 +0% 6`bXX0001 -3% 6`bXX0010 -6% 6`bXX0011 -9% 6`bXX0100 -12% 6`bXX0101 -15% 6`bXX0110 -18% 6`bXX0111 -21% 6`bXX1000 +24% 6`bXX1001 +21% 6`bXX1010 +18% 6`bXX1011 +15% 6`bXX1100 +12% 6`bXX1101 +9% 6`bXX1110 +6% 6`bXX1111 +3% 1'b0: Valley current sense 1'b1: Peak current sense
5:0	RG_VCORE1_CSM_N	**Adjusts current measurement** [5]: IMAX=1.5V or 1V 1b'0: 1.5V 1b'1: 1V [4]: Enable test mode 6`bXX0000 +0% 6`bXX0001 -3% 6`bXX0010 -6% 6`bXX0011 -9% 6`bXX0100 -12% 6`bXX0101 -15% 6`bXX0110 -18% 6`bXX0111 -21% 6`bXX1000 +24% 6`bXX1001 +21% 6`bXX1010 +18% 6`bXX1011 +15% 6`bXX1100 +12% 6`bXX1101 +9% 6`bXX1110 +6% 6`bXX1111 +3% 1'b0: Disable

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Bit(s)	Name	Description
		1'b1: Enable

0446 **VCORE_ANA_CON3** **VCORE_ANA Control Register 3** **04F0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VCORE1_PFM_RIP			RG_VCORE1_RSV							
Type						RW			RW							
Reset						1	0	0	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
10:8	RG_VCORE1_PFM_RIP	**PFM ripple control bit** 1LSB = 6.25mV 3'b000: +0LSB 3'b001: +1LSB 3'b010: +2LSB 3'b011: +3LSB 3'b100: +4LSB 3'b101: +5LSB 3'b110: +6LSB 3'b111: +7LSB
7:0	RG_VCORE1_RSV	**Reserved:** [7]: For nlim trimmimg [6]: For nlim trimmimg [5]: HS on- speed increase [4]: Power good function gating [3]: HS driver decection threshold voltage [2]: VBAT<2.8V, increase powermos slew rate [1]: nlim gating [0]: In PFM mode, increase slew rate 0: Check output drop voltage (comparator) 1: Check NMOS threshold

0448 **VCORE_ANA_CON4** **VCORE_ANA Control Register 4** **000B**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_VCORE1_DTS_ENB	RG_VCORE1_TRAN_BST					
Type										RW	RW					
Reset										0	0	0	1	0	1	1

Bit(s)	Name	Description
6	RG_VCORE1_DTS_ENB	**Differential to single buffer disable signal**
5:0	RG_VCORE1_TRAN_BST	**PFM -> PWM transient boost EN (1=EN)** [5]: Reserved [4]: Drop

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Bit(s)	Name	Description
		[3:2]: 00: 0 preset duty 01: Preset duty low 10: Preset duty med 11: Preset duty high [1]: AVP [0]: BW extension

044A	VSYS22_ANA_CON0	VSYS22_ANA Control Register 0	0C12

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VSYS22_AUTO_MODE	RG_VSYS22_CSR					RG_VSYS22_RZSEL			RG_VSYS22_1P35UP_SEL_EN	RG_VSYS22_VRF18_SSTART_EN	RG_VSYS22_NVT_BUFF_OFF_EN	RG_VSYS22_MIN_OFF	
Type			RW	RW					RW			RW	RW	RW	RW	
Reset			0	0	1	1			0	0	0	1	0	0	1	0

Bit(s)	Name	Description
13	RG_VSYS22_AUTO_MODE	**Not used**
12:10	RG_VSYS22_CSR	**Adjusts current sense ratio** 3'b000: 234mV 3'b001: 208mV 3'b010: 182mV 3'b011: 156mV (default) 3'b100: 130mV 3'b101: 104mV 3'b110: 78mV 3'b111: 52mV
7:5	RG_VSYS22_RZSEL	**Adjusts compensation R** 3'b000: 700 kohm (default) 3'b001: 300 kohm 3'b010: 200 kohm 3'b011: 500 kohm 3'b100: 800 kohm 3'b101: 900 kohm 3'b110: 1000 kohm 3'b111: 1200 kohm
4	RG_VSYS22_1P35UP_SEL_EN	**Selects Vo>=1.35v** 1'b0: Vo<1.35v 1'b1: Vo>=1.35v
3	RG_VSYS22_VRF18_SSTART_EN	**Enables VSYS22 soft-start time** 1'b0: Disable 1'b1: Enable
2	RG_VSYS22_NVT_BUFF_OFF_EN	**Not used**
1:0	RG_VSYS22_MIN_OFF	**Not used**

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044C	VSYS22_ANA_CON1	VSYS22_ANA Control Register 1	041C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VSYS22_NDIS_EN	RG_VSYS22_MODESET	RG_VSYS22_ZX_OS		RG_VSYS22_SLP			RG_VSYS22_CSL			
Type						RW	RW	RW		RW			RW			
Reset						1	0	0	0	0	0	1	1	1	0	0

Bit(s)	Name	Description
10	RG_VSYS22_NDIS_EN	**Enables NMOS discharge** 1'b1: Enable NMOS discharge (default) 1'b0: Disable NMOS discharge
9	RG_VSYS22_MODESET	**Selects force PWM mode** 1'b1: Force PWM mode 1'b0: Auto mode
8:7	RG_VSYS22_ZX_OS	**nlim offset adjustment combined with RG_VSYS22_RSV[7:6]** RG_VSYS22_RSV[7:6]+RG_VSYS22_ZX_OS[1:0] 1LSB = 170mA 0001: -1LSB 0010: -2LSB 0100: -4LSB 1000: +8LSB
6:4	RG_VSYS22_SLP	**Adjusts slope compensation** 3'b000: 1uA 3'b001: 1.5uA (default) 3'b010: 2uA 3'b011: 2.5uA 3'b100: 3uA 3'b101: 3.5uA 3'b110: 4uA 3'b111: 4.5uA
3:0	RG_VSYS22_CSL	**Adjusts over current limit** 4'b0000: 1.2A 4'b1000: 2A 4'b1100: 3A (default) 4'b1110: 4A 4'b1111: 4.8A

044E	VSYS22_ANA_CON2	VSYS22_ANA Control Register 2	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VSYS22_CSM_P						RG_VSYS22_CSM_N					
Type					RW						RW					
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:6	RG_VSYS22_CSM_P	**Adjusts current measurement** 6`bXX0000 +0%

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Bit(s)	Name	Description
		6`bXX0001 -3% 6`bXX0010 -6% 6`bXX0011 -9% 6`bXX0100 -12% 6`bXX0101 -15% 6`bXX0110 -18% 6`bXX0111 -21% 6`bXX1000 +24% 6`bXX1001 +21% 6`bXX1010 +18% 6`bXX1011 +15% 6`bXX1100 +12% 6`bXX1101 +9% 6`bXX1110 +6% 6`bXX1111 +3%
5:0	RG_VSYS22_CSM_N	**Adjusts current measurement** 6`bXX0000 +0% 6`bXX0001 -3% 6`bXX0010 -6% 6`bXX0011 -9% 6`bXX0100 -12% 6`bXX0101 -15% 6`bXX0110 -18% 6`bXX0111 -21% 6`bXX1000 +24% 6`bXX1001 +21% 6`bXX1010 +18% 6`bXX1011 +15% 6`bXX1100 +12% 6`bXX1101 +9% 6`bXX1110 +6% 6`bXX1111 +3%

0450 **VSYS22_ANA_CON3** **VSYS22_ANA Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VSYS22_ZXOS_TRIM						RG_VSYS22_RSV							
Type			RW						RW							
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:8	RG_VSYS22_ZXOS_TRIM	**LX zero-crossing offset trimming** 1LSB=150mA 6'b000001: +1LSB 6'b000010: +2LSB 6'b000100: +4LSB 6'b001000: -1LSB 6'b010000: -2LSB 6'b100000: -4LSB
7:0	RG_VSYS22_RSV	**Reserved** [7]: For nlim trimmimg [6]: For nlim trimmimg [5]: HS on- speed increase [4]: For power good ibias enable [3]: HS driver decection threshold voltage

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Bit(s)	Name	Description
		[2]: VBAT<2.8V, increase powermos slew rate [1]: nlim gating [0]: In PFM mode, increase slew rate

0452 VSYS22_ANA_CON4 VSYS22_ANA Control Register 4 005A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_VSYS22_DTS_ENB	RG_VSYS22_TRAN_BST						RG_VSYS22_PFM_RIP		
Type							RW	RW						RW		
Reset							0	0	0	1	0	1	1	0	1	0

Bit(s)	Name	Description
9	RG_VSYS22_DTS_ENB	**Differential to single buffer disable signal**
8:3	RG_VSYS22_TRAN_BST	**PFM -> PWM transient boost EN (1=EN)** [5]: Reserved [4]: Drop [3:2]: 00: No preset duty 01: Peset duty low 10: Preset duty med 11: Preset duty high [1]: AVP [0]: BW extension
2:0	RG_VSYS22_PFM_RIP	**PFM ripple control bit** 1LSB = 6.25mV 3'b000: +0LSB 3'b001: +1LSB 3'b010: +2LSB 3'b011: +3LSB 3'b100: +4LSB 3'b101: +5LSB 3'b110: +6LSB 3'b111: +7LSB

0454 VPROC_ANA_CON0 VPROC_ANA Control Register 0 2262

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_VPROC_AUTO_MODE	RG_VPROC_CSL				RG_VPROC_CSR			RG_VPROC_RZSEL			RG_VPROC_1P35UP_SEL_EN	RG_VPROC_VRF18_SSTART_EN	RG_VPROC_MIN_OFF	
Type		RW	RW				RW			RW			RW	RW	RW	
Reset		0	1	0	0	0	1	0	0	1	1	0	0	0	1	0

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Bit(s)	Name	Description
14	RG_VPROC_AUTO_MODE	1'b1: Disable OP tran-boost function 1'b0: Normal
13:10	RG_VPROC_CSL	**Adjusts over current limit** 4'b0000: 8A 4'b1000: 7A(default) 4'b1100: 6A 4'b1110: 5A 4'b1111: 4A
9:7	RG_VPROC_CSR	**Adjusts current sense ratio** 3'b000: 15.75K; 233mV/A 3'b001: 13.5K; 200mV/A 3'b010: 11.25K; 167mV/A 3'b011: 9K; 133mV/A 3'b100: 6.75K (default); 100mV/A 3'b101: 4.5K; 67mV/A 3'b110: 2.25K; 33mV/A 3'b111: 0K
6:4	RG_VPROC_RZSEL	**Adjusts compensation R** 3'b000: 400 kohm 3'b001: 800 kohm 3'b010: 1200 kohm 3'b011: 1400 kohm 3'b100: 1500 kohm 3'b101: 1600 kohm 3'b110: 1800 kohm (default) 3'b111: 1900 kohm
3	RG_VPROC_1P35UP_SEL_EN	**vo>=1.35v** 1'b0: vo<1.35V, valley current sense 1'b1: vo>=1.35V, peak current sense
2	RG_VPROC_VRF18_SSTART_EN	**Not used**
1:0	RG_VPROC_MIN_OFF	**Not used**

0456 **VPROC_ANA_CON1** **VPROC_ANA Control Register 1** **1004**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VCORE1_AUTO_MODE	RG_VPROC_NDIS_EN	RG_VPROC_MODESET	RG_VPROC_ZXOS_TRIM						RG_VPROC_ZX_OS		RG_VPROC_SLP		
Type			RW	RW	RW	RW						RW		RW		
Reset			0	1	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
13	RG_VCORE1_AUTO_MODE	**Not used**
12	RG_VPROC_NDIS_EN	**Enables NMOS discharge** 1'b1: Enable NMOS discharge (default)

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Bit(s)	Name	Description
		1'b0: Disable NMOS discharge
11	RG_VPROC_MODESET	**Selects force PWM mode** 1'b1: Force PWM mode 1'b0: Auto mode
10:5	RG_VPROC_ZXOS_TRIM	**1LSB=260mA** LX zero-crossing offset trimming 6'b000001: +1LSB 6'b000010: +2LSB 6'b000100: +4LSB 6'b001000: -1LSB 6'b010000: -2LSB 6'b100000: -4LSB
4:3	RG_VPROC_ZX_OS	**Nlim trimimg bits(combined with RG_VPROC_RSV[7],[6], as RG_VPROC_RSV[7],[6],zx_os[1],[0])** 2'b0100: -5m 2'b 1000: -1.66 2'b1110: -1.74 2'b1101: -1.62 2'b1100: -1.5
2:0	RG_VPROC_SLP	**Adjusts slope compensation** 3'b000: 1uA 3'b001: 1.5uA 3'b010: 2uA 3'b011: 2.5uA 3'b100: 3uA (default) 3'b101: 3.5uA 3'b110: 4uA 3'b111: 4.5uA

0458 **VPROC_ANA_CON2** **VPROC_ANA Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VPROC_CSM_P						RG_VPROC_CSM_N					
Type					RW						RW					
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:6	RG_VPROC_CSM_P	**Adjusts current measurement** [0]: IMAX=1.5V or 1V 1b'0: 1.5V 1b'1: 1V [5]: Test peak/valley current 1'b0: Valley 1'b1: Peak 6`bXX0000 +0% 6`bXX0001 -3% 6`bXX0010 -6% 6`bXX0011 -9% 6`bXX0100 -12% 6`bXX0101 -15% 6`bXX0110 -18% 6`bXX0111 -21% 6`bXX1000 +24% 6`bXX1001 +21%

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Bit(s)	Name	Description
		6`bXX1010 +18% 6`bXX1011 +15% 6`bXX1100 +12% 6`bXX1101 +9% 6`bXX1110 +6% 6`bXX1111 +3%
5:0	RG_VPROC_CSM_N	**Adjusts current measurement** [0]: IMAX=1.5V or 1V 1b'0: 1.5V 1b'1: 1V [5]: Enable test mode 1'b0: Disable 1'b1: Enable 6`bXX0000 +0% 6`bXX0001 -3% 6`bXX0010 -6% 6`bXX0011 -9% 6`bXX0100 -12% 6`bXX0101 -15% 6`bXX0110 -18% 6`bXX0111 -21% 6`bXX1000 +24% 6`bXX1001 +21% 6`bXX1010 +18% 6`bXX1011 +15% 6`bXX1100 +12% 6`bXX1101 +9% 6`bXX1110 +6% 6`bXX1111 +3%

045A **VPROC_ANA_CON3** **VPROC_ANA Control Register 3** **04F0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_VPROC_PFM_RIP			RG_VPROC_RSV							
Type						RW			RW							
Reset						1	0	0	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
10:8	RG_VPROC_PFM_RIP	**PFM ripple control bit** 1 LSB=6.25mV 3'b000: +0LSB 3'b001: +1LSB 3'b010: +2LSB 3'b011: +3LSB 3'b100: +4LSB 3'b101: +5LSB 3'b110: +6LSB 3'b111: +7LSB
7:0	RG_VPROC_RSV	**Reserved** [7]: For nlim trimming [6]: For nlim trimming [5]: HS on- speed increase [4]: Power good function gating 0: Check output drop voltage (COMPARATOR)

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Bit(s)	Name	Description
		1: Check NMOS threshold [3]: HS driver detection threshold voltage [2]: VBAT<2.8V, increase powermos slew rate [1]: nlim gating [0]: In PFM mode, increase slew rate

045C **VPROC_ANA_CON4** **VPROC_ANA Control Register 4** **000B**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_VPROC_DTS_ENB	RG_VPROC_TRAN_BST					
Type										RW	RW					
Reset										0	0	0	1	0	1	1

Bit(s)	Name	Description
6	RG_VPROC_DTS_ENB	**Differential to single buffer disable signal**
5:0	RG_VPROC_TRAN_BST	**PFM -> PWM transient boost EN (1=EN)** [5]: reserved, no used [4]: reserved, no used [3]:reserved, no used [2]:reserved, no used [1]: AVP [0]: BW extension

045E **OSC32_ANA_CON0** **OSC32 Control Register 0** **3BC7**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_EOSC_LPD_RST	RG_EOSC_LPD_EN	RG_EOSC_CHOP_EN	RG_XOSC_PWDB	RG_EOSC_PWDB	RG_EOSC_CALI					RG_LPD_RESET	RG_LPD_EN	RG_XOSC_CALI			
Type	RW	RW	RW	RW	RW	RW					RW	RW	RW			
Reset	0	0	1	1	1	0	1	1	1	1	0	0	0	1	1	1

Bit(s)	Name	Description
15	RG_EOSC_LPD_RST	**Resets low power detection** 0: Does not reset 1: Reset low power detection output to 1
14	RG_EOSC_LPD_EN	**Enables OSC32 low power detection**
13	RG_EOSC_CHOP_EN	**Enables chopper**
12	RG_XOSC_PWDB	**EOSC PWDB** 0: Power down

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Bit(s)	Name	Description
		1: Power on
11	RG_EOSC_PWDB	**EOSC PWDB** 0: Power down 1: Power on
10:6	RG_EOSC_CALI	**Calibrates charging cap**
5	RG_LPD_RESET	**Resets low power detection** 0: Does not reset 1: Reset low power detection output to 1
4	RG_LPD_EN	**Enables OSC32 low power detection**
3:0	RG_XOSC_CALI	**Calibrates GM** Default: 4'b0111 Setting the 2nd step to 4'b0000 is suggested.

0460 **OSC32_ANA_CON1** **OSC32 Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_EOSC_RSV		RG_EOSC_OPT		RG_EOSC_VCT_EN
Type												RW		RW		RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:3	RG_EOSC_RSV	**EOSC32 RSV**
2:1	RG_EOSC_OPT	**EOSC32 LPD OPT**
0	RG_EOSC_VCT_EN	**Enables EOSC32 threshold tracking** 0: Disable 1: Enable

0462 **VPA_ANA_CON0** **VPA_ANA Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VPA_SLP		RG_VPA_CSL		RG_VPA_CSMIR		RG_VPA_CSR		RG_VPA_CC		RG_VPA_RZSEL	
Type					RW		RW		RW		RW		RW		RW	
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:10	RG_VPA_SLP	**Adjusts slope compensation** 00: 1.5uA (default) 01: 1uA 10: 2.5uA 11: 2uA
9:8	RG_VPA_CSL	**Adjusts over current limit** 00: 1.6A 01: 1.2A

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Bit(s)	Name	Description
		10: 2.0A 11: 2.4A
7:6	RG_VPA_CSMIR	**00: 1.0X** 01: 1.5X 10: 2.0X 11: 2.5X
5:4	RG_VPA_CSR	**Adjusts current sense ratio** 00: 1x (default) 01: 0.5x 10: 1.25x 11: 0.75x
3:2	RG_VPA_CC	**Adjusts compensation C** 00: 8pF (default) 01: 6pF 10: 3pF 11: 1pF
1:0	RG_VPA_RZSEL	**Adjusts compensation R** 00: 900kohm (default) 01: 700kohm 10: 1.1Mohm 11: 1.3Mohm

0464 VPA_ANA_CON1 VPA_ANA Control Register 1 8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VPA_NDIS_EN	RG_VPA_SLEW_NMOS		RG_VPA_SLEW		RG_VPA_MODESET	RG_VPA_BWEX_GAT	RG_VPA_HZP	RG_VPA_ZX_OS		RG_VPA_ZX_OS_TRIM					
Type	RW	RW		RW		RW	RW	RW	RW		RW					
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RG_VPA_NDIS_EN	**Enables power down NMOS**
14:13	RG_VPA_SLEW_NMOS	**Controls lgate slew rate** 00: ~1ns (default) 01: ~2ns 10: ~5ns 11: ~10ns
12:11	RG_VPA_SLEW	**Controls ugate slew rate** 00: ~1ns (default) 01: ~2ns 10: ~5ns 11: ~10ns
10	RG_VPA_MODESET	**0: Auto mode** 1: Force PWM mode
9	RG_VPA_BWEX_GAT	**BW extension function gating** 0: BW extension on (default) 1: BW extension off
8	RG_VPA_HZP	**HZ prevention function gating** 0: HZ prevention on (default)

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Bit(s)	Name	Description
		1: HZ prevention off
7:6	RG_VPA_ZX_OS	**Adjusts positive offset for LX zero-crossing detection** 00: +200mV (default) 01: +150mV 10: +250mV 11: +300mV
5:0	RG_VPA_ZX_OS_TRIM	**Adjusts offset for LX zero-crossing detection** 0000: -200mV (default) 0001: -150mV 0010: -250mV 0011: -300mV 1101: -800mV 1111: -850mV

0466 **VPA_ANA_CON2** **VPA_ANA Control Register 2** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_VPA_RSV1								RG_VPA_EN	RG_VPA_VBAT_DEL		RG_VPA_MIN_ON	
Type				RW								RW	RW		RW	
Reset				0	0	0	0	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
12:5	RG_VPA_RSV1	**RG_VPA_RSV[0]: BW extension gating** RG_VPA_RSV[4:1]: Zero crossing detection point adjustment RG_VPA_RSV[5]: HZ prevention gating RG_VPA_RSV[6]: CS adjustment
4	RG_VPA_EN	**V3GPA enable signal** 0: Disable 1: Enable
3:2	RG_VPA_VBAT_DEL	**Detects lowdrop out threshold** 00: VR=0.6V (default) 01: VR=0.55V 10: VR=0.65V 11: VR=0.70V
1:0	RG_VPA_MIN_ON	

0468 **VPA_ANA_CON3** **VPA_ANA Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_VPA_RSV2							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RG_VPA_RSV2	**RG_VPA_RSV[0]: BW extension gating** RG_VPA_RSV[4:1]: Zero crossing detection point adjustment RG_VPA_RSV[5]: HZ prevention gating

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Bit(s)	Name	Description
		RG_VPA_RSV[6]: CS adjustment

046A VLTE_ANA_CON0 VLTE_ANA Control Register 0 32A2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VLTE_CSL				RG_VLTE_CSR			RG_VLTE_RZSEL			RG_VLTE_1P35UP_SEL_EN	RG_VLTE_VRF18_SSTART_EN	RG_VLTE_MIN_OFF	
Type			RW				RW			RW			RW	RW	RW	
Reset			1	1	0	0	1	0	1	0	1	0	0	0	1	0

Bit(s)	Name	Description
13:10	RG_VLTE_CSL	**Over current limit adjustment** 4'b0000: 3.6A 4'b0001: 3.7A 4'b0010: 3.8A 4'b0011: 4A 4'b0100: 4.2A 4'b0101: 4.4A 4'b0110: 4.6A 4'b0111: 4.8A 4'b1000: 5A 4'b1001: 5.3A 4'b1010: 5.6A 4'b1011: 6A 4'b1100: 6.4A 4'b1101: 6.9A 4'b1110: 7.4A 4'b1111: 8A 4'b0000: 3.6A 4'b0001: 3.7A 4'b0010: 3.8A 4'b0011: 4A 4'b0100: 4.2A 4'b0101: 4.4A 4'b0110: 4.6A 4'b0111: 4.8A 4'b1000: 5A 4'b1001: 5.3A 4'b1010: 5.6A 4'b1011: 6A 4'b1100: 6.4A 4'b1101: 6.9A 4'b1110: 7.4A 4'b1111: 8A
9:7	RG_VLTE_CSR	**Current sense ratio adjustment** 3'b000: 18K (800mV) 3'b001: 15.75K (700mV) 3'b010:13.5K (600mV) 3'b011: 11.25K (500mV) 3'b100: 9K (400mV) 3'b101: 6.75K (300mV)

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Bit(s)	Name	Description
		3'b110: 4.5K (200mV) 3'b111: 2.25K (100mV) 3'b000: 18K (800mV) 3'b001: 15.75K (700mV) 3'b010: 13.5K (600mV) 3'b011: 11.25K (500mV) 3'b100: 9K (400mV) 3'b101: 6.75K (300mV) 3'b110: 4.5K (200mV) 3'b111: 2.25K (100mV)
6:4	RG_VLTE_RZSEL	**Compensation R adjustment** 3'b000: 300 kohm 3'b001: 500 kohm 3'b010: 600 kohm 3'b011: 700 kohm 3'b100: 800 kohm 3'b101: 900 kohm 3'b110: 1000 kohm 3'b111: 1200 kohm 3'b000: 300 kohm 3'b001: 500 kohm 3'b010: 600 kohm 3'b011: 700 kohm 3'b100: 800 kohm 3'b101: 900 kohm 3'b110: 1000 kohm 3'b111: 1200 kohm
3	RG_VLTE_1P35UP_SEL_EN	**Rdiv select** 1'b0: vo<1.35v 1'b1: vo>=1.35v 1'b0: vo<1.35v 1'b1: vo>=1.35v
2	RG_VLTE_VRF18_SSTART_EN	**Not used**
1:0	RG_VLTE_MIN_OFF	**Not used**

046C **VLTE_ANA_CON1** VLTE_ANA Control Register 1 101A

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**RG_VLTE_AUTO_MODE**	**RG_VLTE_NDIS_EN**	**RG_VLTE_MODESET**	**RG_VLTE_ZXOS_TRIM**						**RG_VLTE_ZX_OS**		**RG_VLTE_SLP**		
Type			RW	RW	RW	RW						RW		RW		
Reset			0	1	0	0	0	0	0	0	0	1	1	0	1	0

Bit(s)	Name	Description
13	RG_VLTE_AUTO_MODE	**no used**
12	RG_VLTE_NDIS_EN	**Enables NMOS discharge** 1'b1: Enable NMOS discharge (default)

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Bit(s)	Name	Description
		1'b0: Disable NMOS discharge
11	RG_VLTE_MODESET	**Selects force PWM mode** 1'b1: Force PWM mode 1'b0: Auto mode
10:5	RG_VLTE_ZXOS_TRIM	**1LSB=170mA** LX zero-crossing offset trimming 6'b000001: +1LSB 6'b000010: +2LSB 6'b000100: +4LSB 6'b001000: -1LSB 6'b010000: -2LSB 6'b100000: -4LSB
4:3	RG_VLTE_ZX_OS	**nlim offset adjustment combine with RG_VLTE_RSV[7:6]** RG_VLTE_RSV[7:6]+RG_VLTE_ZX_OS[1:0] 1LSB = 175mA 1110: -1LSB 1101: -2LSB 1011: -4LSB 0111: +8LSB
2:0	RG_VLTE_SLP	**Adjusts slope compensation** 3'b000: 2.0u 3'b001: 2.5u 3'b010: 3.0u 3'b011: 3.5u 3'b100: 4.0u 3'b101: 4.5u 3'b110: 5.0u 3'b111: 5.5u

046E **VLTE_ANA_CON2** **VLTE_ANA Control Register 2** **0820**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VLTE_CSM_P						RG_VLTE_CSM_N					
Type					RW						RW					
Reset					1	0	0	0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
11:6	RG_VLTE_CSM_P	**Adjusts current measurement** [5]: IMAX=1.5V or 1V 1b'0: 1.5V 1b'1: 1V [4]: Enable test mode 1'b0: Valley current sense 1'b1: Peak current sense 6`bXX0000 +0% 6`bXX0001 -3% 6`bXX0010 -6% 6`bXX0011 -9% 6`bXX0100 -12% 6`bXX0101 -15% 6`bXX0110 -18% 6`bXX0111 -21% 6`bXX1000 +24% 6`bXX1001 +21%

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Bit(s)	Name	Description
		6`bXX1010 +18% 6`bXX1011 +15% 6`bXX1100 +12% 6`bXX1101 +9% 6`bXX1110 +6% 6`bXX1111 +3%
5:0	RG_VLTE_CSM_N	**Adjusts current measurement** [5]: IMAX=1.5V or 1V 1b'0: 1.5V 1b'1: 1V [4]: Enable test mode 1'b0: Disable 1'b1: Enable 6`bXX0000 +0% 6`bXX0001 -3% 6`bXX0010 -6% 6`bXX0011 -9% 6`bXX0100 -12% 6`bXX0101 -15% 6`bXX0110 -18% 6`bXX0111 -21% 6`bXX1000 +24% 6`bXX1001 +21% 6`bXX1010 +18% 6`bXX1011 +15% 6`bXX1100 +12% 6`bXX1101 +9% 6`bXX1110 +6% 6`bXX1111 +3%

0470 VLTE_ANA_CON3 VLTE_ANA Control Register 3 04F0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**RG_VLTE_PFM_RIP**			**RG_VLTE_RSV**							
Type						RW			RW							
Reset						1	0	0	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
10:8	RG_VLTE_PFM_RIP	**PFM ripple control bit** 1LSB = 6.25mV 3'b000: +0LSB 3'b001: +1LSB 3'b010: +2LSB 3'b011: +3LSB 3'b100: +4LSB 3'b101: +5LSB 3'b110: +6LSB 3'b111: +7LSB
7:0	RG_VLTE_RSV	**Reserved** [7]: For nlim trimmimg [6]: For nlim trimmimg [5]: HS on- speed increase [4]: Power good function gating 0: Check output drop voltage (comparator)

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Bit(s)	Name	Description
		1: Check NMOS threshold [3]: HS driver detection threshold voltage [2]: VBAT<2.8V, increase powermos slew rate [1]: nlim gating [0]: In PFM mode, increase slew rate

0472 VLTE_ANA_CON4 VLTE_ANA Control Register 4 000B

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_VLTE_DTS_ENB	RG_VLTE_TRAN_BST					
Type										RW	RW					
Reset										0	0	0	1	0	1	1

Bit(s)	Name	Description
6	RG_VLTE_DTS_ENB	**Differential to single buffer disable signal**
5:0	RG_VLTE_TRAN_BST	**PFM -> PWM transient boost EN (1=EN)** [5]: Reserved [4]: Drop [3:2]: 00: 0 preset duty 01: Preset duty low 10: Preset duty med 11: Preset duty high [1]: AVP [0]: BW extension

048A VPROC_CON11 VPROC Control Register 11 0058

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VPROC_VOSEL						
Type										RW						
Reset										1	0	1	1	0	0	0

Bit(s)	Name	Description
6:0	VPROC_VOSEL	**Selects VOUT in SW mode** Voltage = 0.6+0.00625*step

04B2 VSRAM_CON11 VSRAM Control Register 11 0060

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VSRAM_VOSEL_RSV						
Type										RW						
Reset										1	1	0	0	0	0	0

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Bit(s)	Name	Description
6:0	VSRAM_VOSEL_RSV	Not used

04DA **VLTE_CON11** **VLTE Control Register 11** **0048**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VLTE_VOSEL						
Type										RW						
Reset										1	0	0	1	0	0	0

Bit(s)	Name	Description
6:0	VLTE_VOSEL	**Voltage= 0.6+0.00625*step**

0616 **VCORE1_CON11** **VCORE1 Control Register 11** **0058**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VCORE1_VOSEL						
Type										RW						
Reset										1	0	1	1	0	0	0

Bit(s)	Name	Description
6:0	VCORE1_VOSEL	**Selects VOUT in SW mode** Voltage = 0.6+0.00625*step

063E **VSYS22_CON11** **VSYS22 Control Register 11** **0040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VSYS22_VOSEL						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	VSYS22_VOSEL	**Selects VOUT in SW mode** Voltage = 1.4+0.00625*step

0666 **VPA_CON11** **VPA Control Register 11** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											VPA_VOSEL					
Type											RW					
Reset											0	0	0	0	0	0

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Bit(s)	Name	Description
5:0	VPA_VOSEL	**Selects VOUT in SW mode**

0800 ZCD_CON0 ZCD Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_AUDZCDMUXSEL_VAUDP15				RG_AUDZCDTIMEOUTMODESEL	RG_AUDZCDGAINSTEPSIZE		RG_AUDZCDGAINSTEPTIME			RG_AUDZCDENABLE
Type						RW				RW	RW		RW			RW
Reset						0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
10:8	RG_AUDZCDMUXSEL_VAUDP15	**Selects zero crossing detection mux** 000: Left line in and Right line in 001: Headphone L and headphone R 010: Handset 011: IV buffer 100: bypass ZCD 101: Bypass ZCD 110: Bypass ZCD 111: Bypass ZCD
6	RG_AUDZCDTIMEOUTMODESEL	
5:4	RG_AUDZCDGAINSTEPSIZE	**Gain step to change internal gain of ZCD** 00: 1dB 01: 2dB 10: 4dB 11: 8dB
3:1	RG_AUDZCDGAINSTEPTIME	**Gain step time to change internal gain of ZCD** 000: 0us 001: 250us 010: 500us 011: 1ms 100: 2ms 101: 4ms 110: 8ms 111: 16ms
0	RG_AUDZCDENABLE	**Enables zero crossing detection (ZCD)** 0: Disable 1: Enable

0802 ZCD_CON1 ZCD Control Register 1 0F9F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUDLORGAIN							RG_AUDLOLGAIN				
Type					RW							RW				
Reset					1	1	1	1	1			1	1	1	1	1

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Bit(s)	Name	Description
11:7	RG_AUDLORGAIN	00000: +8dB 00001: +7dB 10010: -10dB 11111: -40dB (mute)
4:0	RG_AUDLOLGAIN	00000: +8dB 00001: +7dB 10010: -10dB 11111: -40dB (mute)

0804 ZCD_CON2 ZCD Control Register 2 0F9F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUDHPRGAIN							RG_AUDHPLGAIN				
Type					RW							RW				
Reset					1	1	1	1	1			1	1	1	1	1

Bit(s)	Name	Description
11:7	RG_AUDHPRGAIN	00000: +8dB 00001: +7dB 10010: -10dB 11111: -40dB (mute)
4:0	RG_AUDHPLGAIN	00000: +8dB 00001: +7dB 10010: -10dB 11111: -40dB (mute)

0806 ZCD_CON3 ZCD Control Register 3 001F

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_AUDHSGAIN				
Type												RW				
Reset												1	1	1	1	1

Bit(s)	Name	Description
4:0	RG_AUDHSGAIN	00000: +8dB 00001: +7dB 10010: -10dB 11111: -40dB (mute)

0808 ZCD_CON4 ZCD Control Register 4 0707

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_AUDIVRGAIN								RG_AUDIVLGAIN		
Type						RW								RW		
Reset						1	1	1						1	1	1

Bit(s)	Name	Description
10:8	RG_AUDIVRGAIN	000: +5dB

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Bit(s)	Name	Description
		001: +4dB 010: +3dB 011: +2dB 100: +1dB 101: 0dB 110: -1dB 111: -2dB
2:0	RG_AUDIVLGAIN	000: +5dB 001: +4dB 010: +3dB 011: +2dB 100: +1dB 101: 0dB 110: -1dB 111: -2dB

080A **ZCD_CON5** **ZCD Control Register 5** **3F3F**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_AUDINTGAIN2								RG_AUDINTGAIN1					
Type			RO								RO					
Reset			1	1	1	1	1	1			1	1	1	1	1	1

Bit(s)	Name	Description
13:8	RG_AUDINTGAIN2	
5:0	RG_AUDINTGAIN1	

080C **ISINK0_CON0** **ISINK0 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_DIM0_FSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ISINK_DIM0_FSEL	**Selects ISINK0 dimming frequency** Backlight: (@2MHz) 2: 20kHz 61: 1kHz 311: 200Hz 12499: 5Hz 31249: 2Hz 62499: 1Hz Indicator: (@32kHz) 0: 1kHz 4: 200Hz 199: 5Hz 499: 2Hz 999: 1Hz 1999: 0.5Hz 4999: 0.2Hz 9999: 0.1Hz

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080E **ISINK0_CON1** **ISINK0 Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ISINK_CH0_STEP			ISINK_DIM0_DUTY											
Type		RW			RW											
Reset		0	0	0	0	0	0	0	0							

Bit(s)	Name	Description
14:12	ISINK_CH0_STEP	**Coarse 6 step current level for ISINK CH0** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
11:7	ISINK_DIM0_DUTY	**ISINK ON-duty of dimming0 control** N: (N+1)/32 0: 1/32 1: 2/32 2: 3/32 31: 32/32

0810 **ISINK0_CON2** **ISINK0 Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_BREATH0_TR1_SEL				ISINK_BREATH0_TR2_SEL				ISINK_BREATH0_TF1_SEL				ISINK_BREATH0_TF2_SEL			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	ISINK_BREATH0_TR1_SEL	**Selects ISINK0 breath mode rising time for duty 0%~30%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s

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Bit(s)	Name	Description
11:8	ISINK_BREATH0_TR2_SEL	**Selects ISINK0 breath mode rising time for duty 31%~100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
7:4	ISINK_BREATH0_TF1_SEL	**Selects ISINK0 breath mode falling time for duty 0%~30%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	ISINK_BREATH0_TF2_SEL	**Selects ISINK0 breath mode falling time for duty 31%~100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s

0812 **ISINK0_CON3** **ISINK0 Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ISINK_BREATH0_TO								ISINK_BREATH0_TO			

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					N_SEL								FF_SEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	ISINK_BREATH0_TON_SEL	**Selects ISINK0 breath mode Ton time** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	ISINK_BREATH0_TOFF_SEL	**Selects ISINK0 breath mode Toff time** 0: 0.246s 1: 0.677s 2: 1.046s 3: 1.417s 4: 1.845s 5: 2.214s 6: 2.583s 7: 3.014s 8: 3.383s 9: 3.752s 10: 4.183s 11: 4.552s 12: 4.921s 13: 5.351s 14: 5.720s 15: 6.151s

0814 **ISINK1_CON0** **ISINK1 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_DIM1_FSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ISINK_DIM1_FSEL	**Selects ISINK1 dimming frequency** Backlight: (@2MHz) 2: 20kHz 61: 1kHz 311: 200Hz 12499: 5Hz 31249: 2Hz 62499: 1Hz

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Bit(s)	Name	Description
		Indicator: (@32kHz) 0: 1kHz 4: 200Hz 199: 5Hz 499: 2Hz 999: 1Hz 1999: 0.5Hz 4999: 0.2Hz 9999: 0.1Hz

0816 **ISINK1_CON1** **ISINK1 Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ISINK_CH1_STEP			ISINK_DIM1_DUTY											
Type		RW			RW											
Reset		0	0	0	0	0	0	0	0							

Bit(s)	Name	Description
14:12	ISINK_CH1_STEP	**Coarse 6 step current level for ISINK CH1** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
11:7	ISINK_DIM1_DUTY	**ISINK ON-duty of dimming1 control** N: (N+1)/32 0: 1/32 1: 2/32 2: 3/32 31: 32/32

0818 **ISINK1_CON2** **ISINK1 Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_BREATH1_TR1_SEL				ISINK_BREATH1_TR2_SEL				ISINK_BREATH1_TF1_SEL				ISINK_BREATH1_TF2_SEL			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	ISINK_BREATH1_TR1_SEL	**Selects ISINK1 breath mode rising time for duty 0%~30%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s

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Bit(s)	Name	Description
		6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
11:8	ISINK_BREATH1_TR2_SEL	**Selects ISINK1 breath mode rising time for duty 31%~100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
7:4	ISINK_BREATH1_TF1_SEL	**Selects ISINK1 breath mode falling time for duty 0%~30%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	ISINK_BREATH1_TF2_SEL	**Selects ISINK1 breath mode falling time for duty 31%~100%** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s

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Bit(s)	Name	Description
		15: 3.075s

081A ISINK1_CON3 ISINK1 Control Register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ISINK_BREATH1_TON_SEL								ISINK_BREATH1_TOFF_SEL			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	ISINK_BREATH1_TON_SEL	**Selects ISINK1 breath mode Ton time** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0	ISINK_BREATH1_TOFF_SEL	**Selects ISINK1 breath mode Toff time** 0: 0.246s 1: 0.677s 2: 1.046s 3: 1.417s 4: 1.845s 5: 2.214s 6: 2.583s 7: 3.014s 8: 3.383s 9: 3.752s 10: 4.183s 11: 4.552s 12: 4.921s 13: 5.351s 14: 5.720s 15: 6.151s

081C ISINK2_CON1 ISINK2 Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ISINK_CH2_STEP														
Type		RW														

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Reset		0	0	0												

Bit(s)	Name	Description
14:12	ISINK_CH2_STEP	**Coarse 6 step current level for ISINK CH2** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA

081E ISINK3_CON1 ISINK3 Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ISINK_CH3_STEP														
Type		RW														
Reset		0	0	0												

Bit(s)	Name	Description
14:12	ISINK_CH3_STEP	**Coarse 6 step current level for ISINK CH3** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA

0824 ISINK_PHASE_DLY ISINK PHASE DELAY 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ISINK_PHASE_DLY_TC				ISINK_PHASE1_DLY_EN	ISINK_PHASE0_DLY_EN
Type											RW				RW	RW
Reset											0	0			0	0

Bit(s)	Name	Description
5:4	ISINK_PHASE_DLY_TC	**Selects ISINK channel backlight phase delay** Freq: 2MHz/32kHz 2'b00: 1T (0.5us/31.25us) 2'b01: 2T (1us/62.5us) 2'b10: 3T (1.5us/93.75us) 2'b11: 4T (2us/125us)

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Bit(s)	Name	Description
1	ISINK_PHASE1_DLY_EN	**Controls ISINK1 phase delay** 1'b1: Enable phase delay 1'b0: Disable
0	ISINK_PHASE0_DLY_EN	**Controls ISINK0 phase delay** 1'b1: Enable phase delay 1'b0: Disable

0826 ISINK_SFSTR ISINK Soft Start 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ISINK_SFSTR0_TC		ISINK_SFSTR0_EN		ISINK_SFSTR1_TC		ISINK_SFSTR1_EN								
Type		RW		RW		RW		RW								
Reset		0	0	0		0	0	0								

Bit(s)	Name	Description
14:13	ISINK_SFSTR0_TC	**Controls ISINK0 soft start timing step** Freq: 2MHz/32kHz 2'b00: 1T (0.5us/31.25us) 2'b01: 2T (1us/62.5us) 2'b10: 3T (1.5us/93.75us) 2'b11: 4T (2us/125us)
12	ISINK_SFSTR0_EN	**Controls ISINK0 soft start** 1'b1: Enable after start current step 1'b0: Disable
10:9	ISINK_SFSTR1_TC	**Controls ISINK1 soft start timing step** Freq: 2MHz/32kHz 2'b00: 1T (0.5us/31.25us) 2'b01: 2T (1us/62.5us) 2'b10: 3T (1.5us/93.75us) 2'b11: 4T (2us/125us)
8	ISINK_SFSTR1_EN	**Controls ISINK1 soft start** 1'b1: Enable after start current step 1'b0: Disable

0828 ISINK_EN_CTRL ISINK Enable Control 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					ISINK_CH3_BIAS_EN	ISINK_CH2_BIAS_EN	ISINK_CH1_BIAS_EN	ISINK_CH0_BIAS_EN	ISINK_CHOP3_EN	ISINK_CHOP2_EN	ISINK_CHOP1_EN	ISINK_CHOP0_EN	ISINK_CH3_EN	ISINK_CH2_EN	ISINK_CH1_EN	ISINK_CH0_EN
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
11	ISINK_CH3_BIAS_EN	**Enables ISINK Channel 3 bias CLK** 1'b0: Disable 1'b1: Enable
10	ISINK_CH2_BIAS_EN	**Enables ISINK Channel 2 CHOP CLK** 1'b0: Disable 1'b1: Enable
9	ISINK_CH1_BIAS_EN	**Enables ISINK Channel 1 CHOP CLK** 1'b0: Disable 1'b1: Enable
8	ISINK_CH0_BIAS_EN	**Enables ISINK Channel 0 CHOP CLK** 1'b0: Disable 1'b1: Enable
7	ISINK_CHOP3_EN	**Enables ISINK Channel 3 CHOP CLK** 1'b0: Disable 1'b1: Enable
6	ISINK_CHOP2_EN	**Enables ISINK Channel 2 CHOP CLK** 1'b0: Disable 1'b1: Enable
5	ISINK_CHOP1_EN	**Enables ISINK Channel 1 CHOP CLK** 1'b0: Disable 1'b1: Enable
4	ISINK_CHOP0_EN	**Enables ISINK Channel 0 CHOP CLK** 1'b0: Disable 1'b1: Enable
3	ISINK_CH3_EN	**Turns on ISINK Channel 3** 1'b0: Disable 1'b1: Enable
2	ISINK_CH2_EN	**Turns on ISINK Channel 2** 1'b0: Disable 1'b1: Enable
1	ISINK_CH1_EN	**Turns on ISINK Channel 1** 1'b0: Disable 1'b1: Enable
0	ISINK_CH0_EN	**Turns on ISINK Channel 0** 1'b0: Disable 1'b1: Enable

082A **ISINK_MODE_CTRL** **ISINK Mode Control** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_CH0_MODE		ISINK_CH1_MODE													
Type	RW		RW													
Reset	0	0	0	0												

Bit(s)	Name	Description
15:14	ISINK_CH0_MODE	**Selects ISINK Channel 0 enable mode** 2'b00: PWM mode 2'b01: Breath mode

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Bit(s)	Name	Description
		2'b10: Register mode 2'b11: Register mode
13:12	ISINK_CH1_MODE	**Selects ISINK Channel 1 enable mode** 2'b00: PWM mode 2'b01: Breath mode 2'b10: Register mode 2'b11: Register mode

0A00 **VTCXO_0_CON0** **VTCXO_0 Control Register 0** **8102**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VTCXO_0_EN	QI_VTCXO_0_STB			QI_VTCXO_0_OCFB_EN	RG_VTCXO_0_OCFB_EN			QI_VTCXO_0_MODE				RG_VTCXO_0_ON_CTRL	RG_VTCXO_0_MODE_CTRL	RG_VTCXO_0_EN	RG_VTCXO_0_MODE_SET
Type	RO	RO			RO	RW			RO				RW	RW	RW	RW
Reset	1	0			0	0			0				0	0	1	0

Bit(s)	Name	Description
15	QI_VTCXO_0_EN	**VTCXO0 enable status** 1'b1: Enable 1'b0: Disable
14	QI_VTCXO_0_STB	**VTCXO0 soft-start status**
11	QI_VTCXO_0_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VTCXO_0_OCFB_EN	**OCFB Enable** 1'b1: Enable 1'b0: Disable
7	QI_VTCXO_0_MODE	**VTCXO0 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VTCXO_0_ON_CTRL	**VTCXO0 enable control** 1'b0: SW control by RG_VTCXO_0_EN 1'b1: HW control by SRCLKEN
2	RG_VTCXO_0_MODE_CTRL	**VTCXO0 low power mode control** 1'b0: SW control by VTCXO0_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VTCXO_0_EN	**VTCXO0 enable** 1'b1: Dnable 1'b0: Disable
0	RG_VTCXO_0_MODE_SET	**VTCXO0 low power mode** 1'b0: Normal mode 1'b1: Low power mode

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0A02 **VTCXO_1_CON0** **VTCOX_1 Control Register 0** **2120**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VTCXO_1_EN	QI_VTCXO_1_STB			QI_VTCXO_1_OCFB_EN	RG_VTCXO_1_OCFB_EN			QI_VTCXO_1_MODE				RG_VTCXO_1_ON_CTRL	RG_VTCXO_1_MODE_CTRL	RG_VTCXO_1_EN	RG_VTCXO_1_MODE_SET
Type	RO	RO			RO	RW			RO				RW	RW	RW	RW
Reset	0	0			0	0			0				0	0	0	0

Bit(s)	Name	Description
15	QI_VTCXO_1_EN	**VTCXO1 enable status** 1'b1: Enable 1'b0: Disable
14	QI_VTCXO_1_STB	**VTCXO1 soft-start status**
11	QI_VTCXO_1_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VTCXO_1_OCFB_EN	**OCFB Enable** 1'b1: Enable 1'b0: Disable
7	QI_VTCXO_1_MODE	**VTCXO1 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VTCXO_1_ON_CTRL	**VTCXO1 enable control** 1'b0: SW control by RG_VTCXO2_EN 1'b1: HW control by SRCLKEN
2	RG_VTCXO_1_MODE_CTRL	**VTCXO1 low power mode control** 1'b0: SW control by VTCXO1_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VTCXO_1_EN	**VTCXO1 enable** 1'b1: Enable 1'b0: Disable
0	RG_VTCXO_1_MODE_SET	**VTCXO1 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A04 **VAUD28_CON0** **VAUD28 Control Register 0** **8102**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VAUD28_EN	QI_VAUD28_STB			QI_VAUD28_OCFB_EN	RG_VAUD28_OCFB_EN			QI_VAUD28_MODE				RG_VAUD28_ON_CTRL	RG_VAUD28_MODE_CTRL	RG_VAUD28_EN	RG_VAUD28_MODE_SET
Type	RO	RO			RO	RW			RO				RW	RW	RW	RW
Reset	1	0			0	0			0				0	0	1	0

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Bit(s)	Name	Description
15	QI_VAUD28_EN	**VAUD28 enable status** 1'b1: Enable 1'b0: Disable
14	QI_VAUD28_STB	**VAUD28 soft-start status**
11	QI_VAUD28_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VAUD28_OCFB_EN	**OCFB Enable** 1'b1: Enable 1'b0: Disable
7	QI_VAUD28_MODE	**VAUD28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VAUD28_ON_CTRL	**VAUD28 enable control** 1'b0: SW control by RG_VAUD28_EN 1'b1: HW control by SRCLKEN
2	RG_VAUD28_MODE_CTRL	**VAUD28 low power mode control** 1'b0: SW control by VAUD28_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VAUD28_EN	**Enables VAUD28** 1'b1: Enable 1'b0: Disable
0	RG_VAUD28_MODE_SET	**VAUD28 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A06 **VAUX18_CON0** **VAUX18 Control Register 0** **8102**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VAUX18_EN	QI_VAUX18_STB			QI_VAUX18_OCFB_EN	RG_VAUX18_OCFB_EN			QI_VAUX18_MODE				RG_VAUX18_ON_CTRL	RG_VAUX18_MODE_CTRL	RG_VAUX18_EN	RG_VAUX18_MODE_SET
Type	RO	RO			RO	RW			RO				RW	RW	RW	RW
Reset	1	0			0	0			0				0	0	1	0

Bit(s)	Name	Description
15	QI_VAUX18_EN	**VAUX18 enable status** 1'b1: Enable 1'b0: Disable
14	QI_VAUX18_STB	**VAUX18 soft-start status**
11	QI_VAUX18_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VAUX18_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable
7	QI_VAUX18_MOD	**VAUX18 low power mode status**

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Bit(s)	Name	Description
	E	1'b0: Normal mode 1'b1: Low power mode
3	RG_VAUX18_ON_CTRL	**VAUX18 enable control** 1'b0: SW control by RG_VAUXA28_EN 1'b1: HW control by SRCLKEN
2	RG_VAUX18_MODE_CTRL	**VAUX18 low power mode control** 1'b0: SW control by VAUXA28_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VAUX18_EN	**Enables VAUX18** 1'b1: Enable 1'b0: Disable
0	RG_VAUX18_MODE_SET	**VAUX18 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A08 **VRF18_0_CON0** **VRF18_0 Control Register 0** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VRF18_0_EN	QI_VRF18_0_STB			QI_VRF18_0_OCFB_EN	RG_VRF18_0_OCFB_EN			QI_VRF18_0_MODE				RG_VRF18_0_ON_CTRL	RG_VRF18_0_MODE_CTRL	RG_VRF18_0_EN	RG_VRF18_0_MODE_SET
Type	RO	RO			RO	RW			RO				RW	RW	RW	RW
Reset	0	0			0	0			0				0	0	0	0

Bit(s)	Name	Description
15	QI_VRF18_0_EN	**VRF18_0 enable status** 1'b1: Enable 1'b0: Disable
14	QI_VRF18_0_STB	**VRF18_0 soft-start status**
11	QI_VRF18_0_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VRF18_0_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable
7	QI_VRF18_0_MODE	**VRF18_0 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VRF18_0_ON_CTRL	**VRF18_0 enable control** 1'b0: SW control by RG_VBIF28_EN 1'b1: HW control by SRCLKEN
2	RG_VRF18_0_MODE_CTRL	**VRF18_0 low power mode control** 1'b0: SW control by VBIF28_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VRF18_0_EN	**Enables VRF18_0** 1'b1: Enable

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Bit(s)	Name	Description
		1'b0: Disable
0	RG_VRF18_0_MODE_SET	**VRF18_0 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A0A **VRF18_0_CON1** **VRF18_0 Control Register 1** **5000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VRF18_0_FAST_TRAN_EN			RG_VRF18_0_FAST_TRAN_EN												
Type	RO			RW												
Reset	0			1												

Bit(s)	Name	Description
15	QI_VRF18_0_FAST_TRAN_EN	**Fast transient enable status**
12	RG_VRF18_0_FAST_TRAN_EN	**Enables fast transient** 1'b1: Enable 1'b0: Disable

0A0C **VCAMA_CON0** **VCAMA Control Register 0** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VCAMA_EN	QI_VCAMA_STB			QI_VCAMA_OCFB_EN	RG_VCAMA_OCFB_EN									RG_VCAMA_EN	
Type	RO	RO			RO	RW									RW	
Reset	0	0			0	0									0	

Bit(s)	Name	Description
15	QI_VCAMA_EN	**Enables VCAMA** 1'b1: Enable 1'b0: Disable
14	QI_VCAMA_STB	**VCAMA soft-start status**
11	QI_VCAMA_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VCAMA_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable

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Bit(s)	Name	Description
1	RG_VCAMA_EN	**Enables VCAMA** 1'b1: Enable 1'b0: Disable

0A0E	VCN28_CON0	VCN28 Control Register 0	0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VCN28_EN	QI_VCN28_STB			QI_VCN28_OCFB_EN	RG_VCN28_OCFB_EN			QI_VCN28_MODE				RG_VCN28_ON_CTRL	RG_VCN28_MODE_CTRL	RG_VCN28_EN	RG_VCN28_MODE_SET
Type	RO	RO			RO	RW			RO				RW	RW	RW	RW
Reset	0	0			0	0			0				0	0	0	0

Bit(s)	Name	Description
15	QI_VCN28_EN	**VCN28 enable status** 1'b1: Enable 1'b0: Disable
14	QI_VCN28_STB	**VCN28 soft-start status**
11	QI_VCN28_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VCN28_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable
7	QI_VCN28_MODE	**VCN28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VCN28_ON_CTRL	**VCN28 enable control** 1'b0: SW control by RG_VCN28_EN 1'b1: HW control by SRCLKEN
2	RG_VCN28_MODE_CTRL	**VCN28 low power mode control** 1'b0: SW control by VCN28_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VCN28_EN	**Enables VCN28** 1'b1: Enable 1'b0: Disable
0	RG_VCN28_MODE_SET	**VCN28 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A10	VCN33_CON0	VCN33 Control Register 0	0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VCN	QI_VCN			QI_VCN	RG_VCN			QI_VCN					RG_VCN		RG_VCN

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	33_EN	33_STB			33_OCFB_EN	33_OCFB_EN			33_MODE					33_MODE_CTRL		33_MODE_SET
Type	RO	RO			RO	RW			RO					RW		RW
Reset	0	0			0	0			0					0		0

Bit(s)	Name	Description
15	QI_VCN33_EN	**VCN33 enable status** 1'b1: Enable 1'b0: Disable
14	QI_VCN33_STB	**VCN33 soft-start status**
11	QI_VCN33_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VCN33_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable
7	QI_VCN33_MODE	**VCN33 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
2	RG_VCN33_MODE_CTRL	**VCN33 low power mode control** 1'b0: SW control by VCN33_MODE_SET 1'b1: HW control by SRCLKEN
0	RG_VCN33_MODE_SET	**VCN33 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A12 VCN33_CON1 VCN33 Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VCN33_SRCLK_EN_SEL_WIFI										RG_VCN33_ON_CTRL_WIFI		RG_VCN33_EN_WIFI	
Type			RW										RW		RW	
Reset			0	0									0		0	

Bit(s)	Name	Description
13:12	RG_VCN33_SRCLK_EN_SEL_WIFI	**Selects HW srclk enable** 2'b00: SRCLKEN_IN0 2'b01: SRCLKEN_IN1 2'b10: SRCLKEN_IN0 or SRCLKEN_IN1 2'b11: SRCLKEN_IN0 and SRCLKEN_IN1
3	RG_VCN33_ON_CTRL_WIFI	**VCN33 enable control** 1'b0: SW control by RG_VCN33_EN 1'b1: HW control by SRCLKEN
1	RG_VCN33_EN_WIFI	**Enables VCN33** 1'b1: Enable

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Bit(s)	Name	Description
		1'b0: Disable

0A14 VCN33_CON2 VCN33 Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VCN33_SRCLK_EN_SEL_BT										RG_VCN33_ON_CTRL_BT		RG_VCN33_EN_BT	
Type			RW										RW		RW	
Reset			0	0									0		0	

Bit(s)	Name	Description
13:12	RG_VCN33_SRCLK_EN_SEL_BT	**Selects HW srclk enable** 2'b00: SRCLKEN_IN0 2'b01: SRCLKEN_IN1 2'b10: SRCLKEN_IN0 or SRCLKEN_IN1 2'b11: SRCLKEN_IN0 and SRCLKEN_IN1
3	RG_VCN33_ON_CTRL_BT	**VCN33 BT enable control** 1'b0: SW control by RG_VCN33_EN 1'b1: HW control by SRCLKEN
1	RG_VCN33_EN_BT	**Enables VCN33 BT** 1'b1: Enable 1'b0: Disable

0A16 VRF18_1_CON0 VRF18_1 Control Register 0 0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VRF18_1_EN	QI_VRF18_1_STB			QI_VRF18_1_OCFB_EN	RG_VRF18_1_OCFB_EN			QI_VRF18_1_MODE				RG_VRF18_1_ON_CTRL	RG_VRF18_1_MODE_CTRL	RG_VRF18_1_EN	RG_VRF18_1_MODE_SET
Type	RO	RO			RO	RW			RO				RW	RW	RW	RW
Reset	0	0			0	0			0				0	0	0	0

Bit(s)	Name	Description
15	QI_VRF18_1_EN	**VRF18_1 enable status** 1'b1: Enable 1'b0: Disable
14	QI_VRF18_1_STB	**VRF18_1 soft-start status**
11	QI_VRF18_1_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VRF18_1_OCF	**Enables OCFB**

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Bit(s)	Name	Description
	B_EN	1'b1: Enable 1'b0: Disable
7	QI_VRF18_1_MODE	**VRF18_1 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VRF18_1_ON_CTRL	**VRF18_1 enable control** 1'b0: SW control by RG_VRF18_1_EN 1'b1: HW control by SRCLKEN
2	RG_VRF18_1_MODE_CTRL	**VRF18_1 low power mode control** 1'b0: SW control by VRF18_1_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VRF18_1_EN	**Enables VRF18_1** 1'b1: Enable 1'b0: Disable
0	RG_VRF18_1_MODE_SET	**VRF18_1 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A18 **VRF18_1_CON1** **VRF18_1 Control Register 1** **5000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VRF18_1_FAST_TRAN_EN			RG_VRF18_1_FAST_TRAN_EN												
Type	RO			RW												
Reset	0			1												

Bit(s)	Name	Description
15	QI_VRF18_1_FAST_TRAN_EN	**Fast transient enable status**
12	RG_VRF18_1_FAST_TRAN_EN	**Enables fast transient** 1'b1: Enable 1'b0: Disable

0A1A **VUSB33_CON0** **USB33 Control Register 0** **8102**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VUSB33_EN	QI_VUSB33_STB			QI_VUSB33_OCFB_EN	RG_VUSB33_OCFB_EN			QI_VUSB33_MODE				RG_VUSB33_ON_CTRL	RG_VUSB33_MODE_CTRL	RG_VUSB33_EN	RG_VUSB33_MODE_SET
Type	RO	RO			RO	RW			RO				RW	RW	RW	RW
Reset	1	0			0	0			0				0	0	1	0

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Bit(s)	Name	Description
15	QI_VUSB33_EN	**VUSB33 enable status** 1'b1: Enable 1'b0: Disable
14	QI_VUSB33_STB	**VSUB33 soft-start status**
11	QI_VUSB33_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VUSB33_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable
7	QI_VUSB33_MODE	**VUSB33 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VUSB33_ON_CTRL	**VUSB33 enable control** 1'b0: SW control by RG_VUSB33_EN 1'b1: HW control by SRCLKEN
2	RG_VUSB33_MODE_CTRL	**VUSB33 low power mode control** 1'b0: SW control by VUSB33_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VUSB33_EN	**Enables VUSB33** 1'b1: Enable 1'b0: Disable
0	RG_VUSB33_MODE_SET	**VUSB33 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A1C **VMCH_CON0** **VMCH Control Register 0** **8102**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VMCH_EN	QI_VMCH_STB			QI_VMCH_OCFB_EN	RG_VMCH_OCFB_EN			QI_VMCH_MODE				RG_VMCH_ON_CTRL	RG_VMCH_MODE_CTRL	RG_VMCH_EN	RG_VMCH_MODE_SET
Type	RO	RO			RO	RW			RO				RW	RW	RW	RW
Reset	1	0			0	0			0				0	0	1	0

Bit(s)	Name	Description
15	QI_VMCH_EN	**VMCH enable status** 1'b1: Enable 1'b0: Disable
14	QI_VMCH_STB	**VMCH soft-start status**
11	QI_VMCH_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VMCH_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable

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Bit(s)	Name	Description
7	QI_VMCH_MODE	**VMCH low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VMCH_ON_CTRL	**VMCH enable control** 1'b0: SW control by RG_VMCH_EN 1'b1: HW control by SRCLKEN
2	RG_VMCH_MODE_CTRL	**VMCH low power mode control** 1'b0: SW control by VMCH_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VMCH_EN	**Enables VMCH** 1'b1: Enable 1'b0: Disable
0	RG_VMCH_MODE_SET	**VMCH low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A1E **VMCH_CON1** **VMCH Control Register 1** **5000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VMCH_FAST_TRAN_EN			RG_VMCH_FAST_TRAN_EN												
Type	RO			RW												
Reset	0			1												

Bit(s)	Name	Description
15	QI_VMCH_FAST_TRAN_EN	**Fast transient enable status**
12	RG_VMCH_FAST_TRAN_EN	**Enables fast transient** 1'b1: Enable 1'b0: Disable

0A20 **VMC_CON0** **VMC Control Register 0** **8102**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VMC_EN	QI_VMC_STB			QI_VMC_OCFB_EN	RG_VMC_OCFB_EN			QI_VMC_MODE				RG_VMC_ON_CTRL	RG_VMC_MODE_CTRL	RG_VMC_EN	RG_VMC_MODE_SET
Type	RO	RO			RO	RW			RO				RW	RW	RW	RW
Reset	1	0			0	0			0				0	0	1	0

Bit(s)	Name	Description
15	QI_VMC_EN	**VMC enable status**

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Bit(s)	Name	Description
		1'b1: Enable 1'b0: Disable
14	QI_VMC_STB	**VMC soft-start status**
11	QI_VMC_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VMC_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable
7	QI_VMC_MODE	**VMC low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VMC_ON_CTRL	**VMC enable control** 1'b0: SW control by RG_VMC_EN 1'b1: HW control by SRCLKEN
2	RG_VMC_MODE_CTRL	**VMC low power mode control** 1'b0: SW control by VMC_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VMC_EN	**Enables VMC** 1'b1: Enable 1'b0: Disable
0	RG_VMC_MODE_SET	**VMC low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A22 **VMC_CON1** **VMC Control Register 1** **001B**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RG_VMC_TRANS_EN**
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_VMC_TRANS_EN	**Controls pulse generation** 1'b0: Disable 1'b1: Enable

0A24 **VEMC_3V3_CON0** **VEMC_3V3 Control Register 0** **8102**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**QI_VEMC_3V3_EN**	**QI_VEMC_3V3_STB**			**QI_VEMC_3V3_OCFB_E**	**RG_VEMC_3V3_OCFB_E**			**QI_VEMC_3V3_MODE**				**RG_VEMC_3V3_ON_CTR**	**RG_VEMC_3V3_MODE_C**	**RG_VEMC_3V3_EN**	**RG_VEMC_3V3_MODE_S**

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					N	N							L	TRL		ET
Type	RO	RO			RO	RW			RO				RW	RW	RW	RW
Reset	1	0			0	0			0				0	0	1	0

Bit(s)	Name	Description
15	QI_VEMC_3V3_EN	**VEMC33 enable status** 1'b1: Enable 1'b0: Disable
14	QI_VEMC_3V3_STB	**VEMC33 soft-start status**
11	QI_VEMC_3V3_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VEMC_3V3_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable
7	QI_VEMC_3V3_MODE	**VEMC33 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VEMC_3V3_ON_CTRL	**VEMC33 enable control** 1'b0: SW control by RG_VEMC33_EN 1'b1: HW control by SRCLKEN
2	RG_VEMC_3V3_MODE_CTRL	**VEMC33 low power mode control** 1'b0: SW control by VEMC33_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VEMC_3V3_EN	**Enables VEMC33** 1'b1: Enable 1'b0: Disable
0	RG_VEMC_3V3_MODE_SET	**VEMC33 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A26 **VEMC_3V3_CON1** **VEMC_3V3 Control Register 1** **5000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**QI_VEMC_3V3_FAST_TRAN_EN**			**RG_VEMC_3V3_FAST_TRAN_EN**												
Type	RO			RW												
Reset	0			1												

Bit(s)	Name	Description
15	QI_VEMC_3V3_FAST_TRAN_EN	**Fast transient enable status**
12	RG_VEMC_3V3_FAST_TRAN_EN	**Enables fast transient** 1'b1: Enable 1'b0: Disable

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0A28	VIO28_CON0	VIO28 Control Register 0	8122

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VIO28_EN	QI_VIO28_STB			QI_VIO28_OCFB_EN	RG_VIO28_OCFB_EN			QI_VIO28_MODE				RG_VIO28_ON_CTRL	RG_VIO28_MODE_CTRL	RG_VIO28_EN	RG_VIO28_MODE_SET
Type	RO	RO			RO	RW			RO				RW	RW	RW	RW
Reset	1	0			0	0			0				0	0	1	0

Bit(s)	Name	Description
15	QI_VIO28_EN	**VIO28 enable status** 1'b1: Enable 1'b0: Disable
14	QI_VIO28_STB	**VIO28 soft-start status**
11	QI_VIO28_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VIO28_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable
7	QI_VIO28_MODE	**VIO28 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VIO28_ON_CTRL	**VIO28 enable control** 1'b0: SW control by RG_VIO28_EN 1'b1: HW control by SRCLKEN
2	RG_VIO28_MODE_CTRL	**VIO28 low power mode control** 1'b0: SW control by VIO28_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VIO28_EN	**Enables VIO28** 1'b1: Enable 1'b0: Disable
0	RG_VIO28_MODE_SET	**VIO28 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A2A	VCAMAF_CON0	VCAMAF Control Register 0	0120

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VCAMAF_EN	QI_VCAMAF_STB			QI_VCAMAF_OCFB_EN	RG_VCAMAF_OCFB_EN			QI_VCAMAF_MODE					RG_VCAMAF_MODE_CTRL	RG_VCAMAF_EN	RG_VCAMAF_MODE_SET
Type	RO	RO			RO	RW			RO					RW	RW	RW

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Reset	0	0			0	0			0					0	0	0

Bit(s)	Name	Description
15	QI_VCAMAF_EN	**VCAM_AF enable status** 1'b1: Enable 1'b0: Disable
14	QI_VCAMAF_STB	**VCAM_AF soft-start status**
11	QI_VCAMAF_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VCAMAF_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable
7	QI_VCAMAF_MODE	**VCAM_AF low power mode status** 1'b0: Normal mode 1'b1: Low power mode
2	RG_VCAMAF_MODE_CTRL	**VCAM_AF low power mode control** 1'b0: SW control by VCAM_AF_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VCAMAF_EN	**Enables VCAM_AF** 1'b1: Enable 1'b0: Disable
0	RG_VCAMAF_MODE_SET	**VCAM_AF low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A2C **VGP1_CON0** **VGP1 Control Register 0** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**QI_VGP1_EN**	**QI_VGP1_STB**			**QI_VGP1_OCFB_EN**	**RG_VGP1_OCFB_EN**			**QI_VGP1_MODE**				**RG_VGP1_ON_CTRL**	**RG_VGP1_MODE_CTRL**	**RG_VGP1_EN**	**RG_VGP1_MODE_SET**
Type	RO	RO			RO	RW			RO				RW	RW	RW	RW
Reset	0	0			0	0			0				0	0	0	0

Bit(s)	Name	Description
15	QI_VGP1_EN	**VGP1 enable status** 1'b1: Enable 1'b0: Disable
14	QI_VGP1_STB	**VGP1 soft-start status**
11	QI_VGP1_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VGP1_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable
7	QI_VGP1_MODE	**VGP1 low power mode status** 1'b0: Normal mode 1'b1: Low power mode

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Bit(s)	Name	Description
3	RG_VGP1_ON_CTRL	**VGP1 enable control** 1'b0: SW control by RG_VGP1_EN 1'b1: HW control by SRCLKEN
2	RG_VGP1_MODE_CTRL	**VGP1 low power mode control** 1'b0: SW control by VGP1_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VGP1_EN	**Enables VGP1** 1'b1: Enable 1'b0: Disable
0	RG_VGP1_MODE_SET	**VGP1 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A2E **VGP1_CON1** **VGP1 Control Register 1** **5000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VGP1_FAST_TRAN_EN			RG_VGP1_FAST_TRAN_EN												
Type	RO			RW												
Reset	0			1												

Bit(s)	Name	Description
15	QI_VGP1_FAST_TRAN_EN	**Fast transient enable status**
12	RG_VGP1_FAST_TRAN_EN	**Enables fast transient** 1'b1: Enable 1'b0: Disable

0A30 **VEFUSE_CON0** **VEFUSE Control Register 0** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VEFUSE_EN	QI_VEFUSE_STB			QI_VEFUSE_OCFB_EN	RG_VEFUSE_OCFB_EN			QI_VEFUSE_MODE					RG_VEFUSE_MODE_CTRL	RG_VEFUSE_EN	RG_VEFUSE_MODE_SET
Type	RO	RO			RO	RW			RO					RW	RW	RW
Reset	0	0			0	0			0					0	0	0

Bit(s)	Name	Description
15	QI_VEFUSE_EN	**VEFUSE enable status** 1'b1: Enable 1'b0: Disable

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Bit(s)	Name	Description
14	QI_VEFUSE_STB	**VEFUSE soft-start status**
11	QI_VEFUSE_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VEFUSE_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable
7	QI_VEFUSE_MODE	**VEFUSE low power mode status** 1'b0: Normal mode 1'b1: Low power mode
2	RG_VEFUSE_MODE_CTRL	**VEFUSE low power mode control** 1'b0: SW control by VEFUSE_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VEFUSE_EN	**Enables VEFUSE** 1'b1: Enable 1'b0: Disable
0	RG_VEFUSE_MODE_SET	**VEFUSE low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A32 **VSIM1_CON0** **VSIM1 Control Register 0** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VSIM1_EN	QI_VSIM1_STB							QI_VSIM1_MODE				RG_VSIM1_ON_CTRL	RG_VSIM1_MODE_CTRL	RG_VSIM1_EN	RG_VSIM1_MODE_SET
Type	RO	RO							RO				RW	RW	RW	RW
Reset	0	0							0				0	0	0	0

Bit(s)	Name	Description
15	QI_VSIM1_EN	**VSIM1 enable status** 1'b1: Enable 1'b0: Disable
14	QI_VSIM1_STB	**VSIM1 soft-start status**
7	QI_VSIM1_MODE	**VSIM1 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VSIM1_ON_CTRL	**VSIM1 enable control** 1'b0: SW control by RG_VSIM1_EN 1'b1: HW control by SRCLKEN
2	RG_VSIM1_MODE_CTRL	**VSIM1 low power mode control** 1'b0: SW control by VSIM1_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VSIM1_EN	**Enables VSIM1** 1'b1: Enable 1'b0: Disable
0	RG_VSIM1_MODE	**VSIM1 low power mode**

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Bit(s)	Name	Description
	_SET	1'b0: Normal mode 1'b1: Low power mode

0A34 VSIM2_CON0 VSIM2 Control Register 0 0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VSIM2_EN	QI_VSIM2_STB			QI_VSIM2_OCFB_EN	RG_VSIM2_OCFB_EN			QI_VSIM2_MODE				RG_VSIM2_ON_CTRL	RG_VSIM2_MODE_CTRL	RG_VSIM2_EN	RG_VSIM2_MODE_SET
Type	RO	RO			RO	RW			RO				RW	RW	RW	RW
Reset	0	0			0	0			0				0	0	0	0

Bit(s)	Name	Description
15	QI_VSIM2_EN	**VSIM2 enable status** 1'b1: Enable 1'b0: Disable
14	QI_VSIM2_STB	**VSIM2 soft-start status**
11	QI_VSIM2_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VSIM2_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable
7	QI_VSIM2_MODE	**VSIM2 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VSIM2_ON_CTRL	**VSIM2 enable control** 1'b0: SW control by RG_VSIM2_EN 1'b1: HW control by SRCLKEN
2	RG_VSIM2_MODE_CTRL	**VSIM2 low power mode control** 1'b0: SW control by VSIM2_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VSIM2_EN	**Enables VSIM2** 1'b1: Enable 1'b0: Disable
0	RG_VSIM2_MODE_SET	**VSIM2 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A36 VIO18_CON0 VIO18 Control Register 0 8102

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VIO18_EN	QI_VIO18_STB			QI_VIO18_OCFB	RG_VIO18_OCFB			QI_VIO18_MODE				RG_VIO18_ON_C	RG_VIO18_MODE	RG_VIO18_EN	RG_VIO18_MODE

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					_EN	_EN							TRL	_CTRL		_SET
Type	RO	RO			RO	RW			RO				RW	RW	RW	RW
Reset	1	0			0	0			0				0	0	1	0

Bit(s)	Name	Description
15	QI_VIO18_EN	**VIO18 enable status** 1'b1: Enable 1'b0: Disable
14	QI_VIO18_STB	**VIO18 soft-start status**
11	QI_VIO18_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VIO18_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable
7	QI_VIO18_MODE	**VIO18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VIO18_ON_CTRL	**VIO18 enable control** 1'b0: SW control by RG_VAUD28_EN 1'b1: HW control by SRCLKEN
2	RG_VIO18_MODE_CTRL	**VIO18 low power mode control** 1'b0: SW control by VAUD28_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VIO18_EN	**Enables VIO18** 1'b1: Enable 1'b0: Disable
0	RG_VIO18_MODE_SET	**VIO18 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A38 <u>VIBR_CON0</u> VIBR Control Register 0 0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**QI_VIBR_EN**	**QI_VIBR_STB**			**QI_VIBR_OCFB_EN**	**RG_VIBR_OCFB_EN**			**QI_VIBR_MODE**					**RG_VIBR_MODE_CTRL**	**RG_VIBR_EN**	**RG_VIBR_MODE_SET**
Type	RO	RO			RO	RW			RO					RW	RW	RW
Reset	0	0			0	0			0					0	0	0

Bit(s)	Name	Description
15	QI_VIBR_EN	**VIBR enable status** 1'b1: Enable 1'b0: Disable
14	QI_VIBR_STB	**VIBR soft-start status**
11	QI_VIBR_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.

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Bit(s)	Name	Description
10	RG_VIBR_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable
7	QI_VIBR_MODE	**VCN18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
2	RG_VIBR_MODE_CTRL	**VCN18 low power mode control** 1'b0: SW control by VCN18_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VIBR_EN	**Enables VIBR** 1'b1: Enable 1'b0: Disable
0	RG_VIBR_MODE_SET	**VCN18 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A3A **VCN18_CON0** **VCN18 Control Register 0** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VCN18_EN	QI_VCN18_STB			QI_VCN18_OCFB_EN	RG_VCN18_OCFB_EN			QI_VCN18_MODE				RG_VCN18_ON_CTRL	RG_VCN18_MODE_CTRL	RG_VCN18_EN	RG_VCN18_MODE_SET
Type	RO	RO			RO	RW			RO				RW	RW	RW	RW
Reset	0	0			0	0			0				0	0	0	0

Bit(s)	Name	Description
15	QI_VCN18_EN	**VCN18 enable status** 1'b1: Enable 1'b0: Disable
14	QI_VCN18_STB	**VCN18 soft-start status**
11	QI_VCN18_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VCN18_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable
7	QI_VCN18_MODE	**VCN18 low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VCN18_ON_CTRL	**VCN18 enable control** 1'b0: SW control by RG_VCN18_EN 1'b1: HW control by SRCLKEN
2	RG_VCN18_MODE_CTRL	**VCN18 low power mode control** 1'b0: SW control by VCN18_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VCN18_EN	**Enables VCN18** 1'b1: Enable

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Bit(s)	Name	Description
		1'b0: Disable
0	RG_VCN18_MODE_SET	**VCN18 low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A3C **VCAM_CON0** **VCMAD Control Register 0** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VCAMD_EN	QI_VCAMD_STB			QI_VCAMD_OCFB_EN	RG_VCAMD_OCFB_EN			QI_VCAMD_MODE					RG_VCAMD_MODE_CTRL	RG_VCAMD_EN	RG_VCAMD_MODE_SET
Type	RO	RO			RO	RW			RO					RW	RW	RW
Reset	0	0			0	0			0					0	0	0

Bit(s)	Name	Description
15	QI_VCAMD_EN	**VCAMD enable status** 1'b1: Enable 1'b0: Disable
14	QI_VCAMD_STB	**VCAMD soft-start status**
11	QI_VCAMD_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VCAMD_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable
7	QI_VCAMD_MODE	**VCAMD low power mode status** 1'b0: Normal mode 1'b1: Low power mode
2	RG_VCAMD_MODE_CTRL	**VCAMD low power mode control** 1'b0: SW control by VCAMD_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VCAMD_EN	**Enables VCAMD** 1'b1: Enable 1'b0: Disable
0	RG_VCAMD_MODE_SET	**VCAMD low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A3E **VCAMIO_CON0** **VCAMIO Control Register 0** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VCAMIO_EN	QI_VCAMIO_STB			QI_VCAMIO_OCFB_	RG_VCAMIO_OCFB_			QI_VCAMIO_MODE					RG_VCAMIO_MODE_	RG_VCAMIO_EN	RG_VCAMIO_MODE_

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					EN	EN								CTR L		SET
Type	RO	RO			RO	RW			RO					RW	RW	RW
Reset	0	0			0	0			0					0	0	0

Bit(s)	Name	Description
15	QI_VCAMIO_EN	**VCAMDIO enable status** 1'b1: Enable 1'b0: Disable
14	QI_VCAMIO_STB	**VCAMDIO soft-start status**
11	QI_VCAMIO_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VCAMIO_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable
7	QI_VCAMIO_MODE	**VCAM_IO low power mode status** 1'b0: Normal mode 1'b1: Low power mode
2	RG_VCAMIO_MODE_CTRL	**VCAM_IO low power mode control** 1'b0: SW control by VCAMD_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VCAMIO_EN	**Enables VCAM_IO** 1'b1: Enable 1'b0: Disable
0	RG_VCAMIO_MODE_SET	**VCAM_IO low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A40 **LDO_VSRAM_CON0** **LDO_VSRAM Control Register 0** **8102**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VSRAM_EN	QI_VSRAM_STB			QI_VSRAM_OCFB_EN	RG_VSRAM_OCFB_EN			QI_VSRAM_MODE				RG_VSRAM_ON_CTRL	RG_VSRAM_MODE_CTRL	RG_VSRAM_EN	RG_VSRAM_MODE_SET
Type	RO	RO			RO	RW			RO				RW	RW	RW	RW
Reset	1	0			0	0			0				0	0	1	0

Bit(s)	Name	Description
15	QI_VSRAM_EN	**VSRAM enable status** 1'b1: Enable 1'b0: Disable
14	QI_VSRAM_STB	**VSRAM soft-start status**
11	QI_VSRAM_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VSRAM_OCFB_EN	**Enables OCFB** 1'b1: Enable

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Bit(s)	Name	Description
		1'b0: Disable
7	QI_VSRAM_MODE	**VSRAM low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VSRAM_ON_CTRL	**VSRAM enable control** 1'b0: SW control by RG_VSRAM_EN 1'b1: HW control by SRCLKEN
2	RG_VSRAM_MODE_CTRL	**VSRAM low power mode control** 1'b0: SW control by VSRAM_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VSRAM_EN	**Enables VSRAM** 1'b1: Enable 1'b0: Disable
0	RG_VSRAM_MODE_SET	**VSRAM low power mode** 1'b0: Normal mode 1'b1: Low power mode

0A42 **LDO_VSRAM_CON1** **LDO_VSRAM Control Register 1** **5000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VSRAM_FAST_TRAN_EN			RG_VSRAM_FAST_TRAN_EN												
Type	RO			RW												
Reset	0			1												

Bit(s)	Name	Description
15	QI_VSRAM_FAST_TRAN_EN	**Fast transient enable status**
12	RG_VSRAM_FAST_TRAN_EN	**Enables fast transient** 1'b1: Enable 1'b0: Disable

0A44 **VTREF_CON0** **VTREF Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_TREF_EN	QI_TREF_STB											RG_TREF_ON_CTRL		RG_TREF_EN	
Type	RO	RO											RW		RW	
Reset	0	0											0		0	

Bit(s)	Name	Description

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Bit(s)	Name	Description
15	QI_TREF_EN	**TREF enable status** 1'b1: Enable 1'b0: Disable
14	QI_TREF_STB	
3	RG_TREF_ON_CTRL	**TREF enable control** 1'b0: SW control by RG_TREF_EN 1'b1: HW control by SRCLKEN
1	RG_TREF_EN	**Enables TREF** 1'b1: Enable 1'b0: Disable

0A46 VM_CON0 VM Control Register 0 8102

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VM_EN	QI_VM_STB			QI_VM_OCFB_EN	RG_VM_OCFB_EN			QI_VM_MODE				RG_VM_ON_CTRL	RG_VM_MODE_CTRL	RG_VM_EN	RG_VM_MODE_SET
Type	RO	RO			RO	RW			RO				RW	RW	RW	RW
Reset	1	0			0	0			0				0	0	1	0

Bit(s)	Name	Description
15	QI_VM_EN	**VM enable status** 1'b1: Enable 1'b0: Disable
14	QI_VM_STB	**VM soft-start status**
11	QI_VM_OCFB_EN	**OCFB status** 1'b1: Over current occurs. 1'b0: No over current occurs.
10	RG_VM_OCFB_EN	**Enables OCFB** 1'b1: Enable 1'b0: Disable
7	QI_VM_MODE	**VM low power mode status** 1'b0: Normal mode 1'b1: Low power mode
3	RG_VM_ON_CTRL	**VM enable control** 1'b0: SW control by RG_VM_EN 1'b1: HW control by SRCLKEN
2	RG_VM_MODE_CTRL	**VM low power mode control** 1'b0: SW control by VM_MODE_SET 1'b1: HW control by SRCLKEN
1	RG_VM_EN	**Enables VM** 1'b1: Enable 1'b0: Disable
0	RG_VM_MODE_SET	**VM low power mode** 1'b0: Normal mode 1'b1: Low power mode

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0A48 VM_CON1 VM Control Register 1 5000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VM_FAST_TRAN_EN			RG_VM_FAST_TRAN_EN												
Type	RO			RW												
Reset	0			1												

Bit(s)	Name	Description
15	QI_VM_FAST_TRAN_EN	**Fast transient enable status**
12	RG_VM_FAST_TRAN_EN	**Enables fast transient** 1'b1: Enable 1'b0: Disable

0A4A VRTC_CON0 VRTC Control Register 0 8002

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VRTC_EN														RG_VRTC_EN	
Type	RO														RW	
Reset	1														1	

Bit(s)	Name	Description
15	QI_VRTC_EN	**VRTC enable status**
1	RG_VRTC_EN	**Enables VRTC** 1'b1: Enable 1'b0: Disable

0A4E ALDO_ANA_CON0 ADLDO Control Register 0 8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VAUX18_NDIS_EN				RG_VAUX18_CAL											
Type	RW				RW											
Reset	1				0	0	0	0								

Bit(s)	Name	Description
15	RG_VAUX18_NDIS_EN	**Enables power down NMOS** 1'b1: Enable 1'b0: Disable)
11:8	RG_VAUX18_CAL	**Calibrates voltage**

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Bit(s)	Name	Description
		(4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: 160mV 4'b1001: 140mV 4'b1010: 120mV 4'b1011: 100mV 4'b1100: 80mV 4'b1101: 60mV 4'b1110: 40mV 4'b1111: 20mV

0A50	ADLDO_ANA_CON1	ADLDO Control Register 1	8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VTCXO_0_NDIS_EN				RG_VTCXO_0_CAL											
Type	RW				RW											
Reset	1				0	0	0	0								

Bit(s)	Name	Description
15	RG_VTCXO_0_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down
11:8	RG_VTCXO_0_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV

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0A52 ADLDO_ANA_CON2 ADLDO Control Register 2 8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VTCXO_1_NDIS_EN				RG_VTCXO_1_CAL											
Type	RW				RW											
Reset	1				0	0	0	0								

Bit(s)	Name	Description
15	RG_VTCXO_1_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down
11:8	RG_VTCXO_1_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV

0A54 ADLDO_ANA_CON3 ADLDO Control Register 3 8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VAUD28_NDIS_EN				RG_VAUD28_CAL											
Type	RW				RW											
Reset	1				0	0	0	0								

Bit(s)	Name	Description
15	RG_VAUD28_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down
11:8	RG_VAUD28_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV

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Bit(s)	Name	Description
		4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV

0A56 **ADLDO_ANA_CON4** **ADLDO Control Register 4** **8000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VCN28_NDIS_EN				RG_VCN28_CAL											
Type	RW				RW											
Reset	1				0	0	0	0								

Bit(s)	Name	Description
15	RG_VCN28_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down
11:8	RG_VCN28_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV

0A58 **ADLDO_ANA_CON5** **ADLDO Control Register 5** **8030**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	RG_VCAMA_NDIS_EN				RG_VCAMA_CAL						RG_VCAMA_VOSEL					
Type	RW				RW						RW					
Reset	1				0	0	0	0			1	1				

Bit(s)	Name	Description
15	RG_VCAMA_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down
11:8	RG_VCAMA_CAL	**Calibrate LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV
5:4	RG_VCAMA_VOSEL	**Selects voltage** 2b'00: 1.5V 2b'01: 1.8V 2b'10: 2.5V 2b'11: 2.8V

0A5A ADLDO_ANA_CON6 ADLDO Control Register 6 8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VCN33_NDIS_EN				RG_VCN33_CAL					RG_VCN33_VOSEL						
Type	RW				RW					RW						
Reset	1				0	0	0	0		0	0	0				

Bit(s)	Name	Description
15	RG_VCN33_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down
11:8	RG_VCN33_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV

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Bit(s)	Name	Description
		4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV
6:4	RG_VCN33_VOSEL	**Selects output voltage** 3'b000: 3.3V 3'b001: 3.4V 3'b010: 3.5V 3'b011: 3.6V

0A5C **ADLDO_ANA_CON7** **ADLDO Control Register 7** **8000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VUSB33_NDIS_EN			RG_VUSB33_CAL												
Type	RW			RW												
Reset	1			0	0	0	0									

Bit(s)	Name	Description
15	RG_VUSB33_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down
12:9	RG_VUSB33_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV

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0A5E **ADLDO_ANA_CON8** **ADLDO Control Register 8** **8030**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VEFUSE_NDIS_EN				RG_VEFUSE_CAL					RG_VEFUSE_VOSEL						
Type	RW				RW					RW						
Reset	1				0	0	0	0		0	1	1				

Bit(s)	Name	Description
15	RG_VEFUSE_NDIS_EN	**Enables power down NMOS** 1'b1: Enable 1'b0: Disable
11:8	RG_VEFUSE_CAL	**Calibrates voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: 160mV 4'b1001: 140mV 4'b1010: 120mV 4'b1011: 100mV 4'b1100: 80mV 4'b1101: 60mV 4'b1110: 40mV 4'b1111: 20mV
6:4	RG_VEFUSE_VOSEL	**Selects output voltage** 3'b011: 1.8V 3'b100: 1.9V 3'b101: 2.0V 3'b110: 2.1V 3'b111: 2.2V

0A60 **ADLDO_ANA_CON9** **ADLDO Control Register 9** **8020**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VSIM1_NDIS_EN				RG_VSIM1_CAL					RG_VSIM1_VOSEL						
Type	RW				RW					RW						
Reset	1				0	0	0	0		0	1	0				

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Bit(s)	Name	Description
15	RG_VSIM1_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down
11:8	RG_VSIM1_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV
6:4	RG_VSIM1_VOSEL	**Output selection signal** 3'b001: 1.7V 3'b010: 1.8V 3'b011: 1.86V 3'b101: 2.76V 3'b110: 3.0V 3'b111: 3.1V

0A62 **ADLDO_ANA_CON10** **ADLDO Control Register 10** **8020**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VSIM2_NDIS_EN				RG_VSIM2_CAL					RG_VSIM2_VOSEL						
Type	RW				RW					RW						
Reset	1				0	0	0	0		0	1	0				

Bit(s)	Name	Description
15	RG_VSIM2_NDIS_EN	**Enables LDO output power-down** 1'b0: Disable output power-down 1'b1: Enable output power-down
11:8	RG_VSIM2_CAL	**Calibrates LDO voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV

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Bit(s)	Name	Description
		4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV
6:4	RG_VSIM2_VOSEL	**Output selection signal** 3'b001: 1.7 V 3'b010: 1.8 V 3'b011: 1.86 V 3'b101: 2.76V 3'b110: 3.0 V 3'b111: 3.1 V

0A64 **ADLDO_ANA_CON11** **ADLDO Control Register 11** **8010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VEMC_3V3_NDIS_EN				RG_VEMC_3V3_CAL						RG_VEMC_3V3_VOSEL					
Type	RW				RW						RW					
Reset	1				0	0	0	0			0	1				

Bit(s)	Name	Description
15	RG_VEMC_3V3_NDIS_EN	**Enables power down NMOS** 1'b1: Enable 1'b0: Disable
11:8	RG_VEMC_3V3_CAL	**Calibrates voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: 160mV 4'b1001: 140mV 4'b1010: 120mV 4'b1011: 100mV 4'b1100: 80mV 4'b1101: 60mV 4'b1110: 40mV 4'b1111: 20mV
5:4	RG_VEMC_3V3_VOSEL	**Selects output voltage** 2b'01: 2.9V 2b'10: 3V 2b'11: 3.3V

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0A66 ADLDO_ANA_CON12 ADLDO Control Register 12 8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VMCH_NDIS_EN				RG_VMCH_CAL						RG_VMCH_VOSEL					
Type	RW				RW						RW					
Reset	1				0	0	0	0			0	0				

Bit(s)	Name	Description
15	RG_VMCH_NDIS_EN	**Enables power down NMOS** 1'b1: Enable 1'b0: Disable
11:8	RG_VMCH_CAL	**Calibrates voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: 160mV 4'b1001: 140mV 4'b1010: 120mV 4'b1011: 100mV 4'b1100: 80mV 4'b1101: 60mV 4'b1110: 40mV 4'b1111: 20mV
5:4	RG_VMCH_VOSEL	**Selects output voltage** (2'b00: 2.9V) 2'b00: 2.9V 2'b01: 3.3V 2'b10: 3.3V

0A68 ADLDO_ANA_CON13 ADLDO Control Register 13 0070

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_ADLDO_RSV_H				RG_ADLDO_RSV_L		
Type										RW				RW		
Reset										1	1	1		0	0	0

Bit(s)	Name	Description
6:4	RG_ADLDO_RSV_H	
2:0	RG_ADLDO_RSV_	

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Bit(s)	Name	Description
	L	

0A6A **DLDO_ANA_CON0** **DLDO Control Register 0** **8010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VMC_NDIS_EN				RG_VMC_CAL						RG_VMC_VOSEL					
Type	RW				RW						RW					
Reset	1				0	0	0	0			0	1				

Bit(s)	Name	Description
15	RG_VMC_NDIS_EN	**Enables power down NMOS** 1'b1: Enable 1'b0: Disable
11:8	RG_VMC_CAL	**Calibrates voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: 160mV 4'b1001: 140mV 4'b1010: 120mV 4'b1011: 100mV 4'b1100: 80mV 4'b1101: 60mV 4'b1110: 40mV 4'b1111: 20mV
5:4	RG_VMC_VOSEL	**Selects output voltage** (2'b01: 2.9V) 2'b00: 1.8V 2'b01: 2.9V 2'b10: 3.0V 2'b11: 3.3V

0A6C **DLDO_ANA_CON1** **DLDO Control Register 1** **8050**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VCAMAF_NDIS_EN				RG_VCAMAF_CAL					RG_VCAMAF_VOSEL						
Type	RW				RW					RW						

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Reset	1				0	0	0	0		1	0	1				

Bit(s)	Name	Description
15	RG_VCAMAF_NDIS_EN	**Enables power down NMOS** 1'b1: Enable 1'b0: Disable
11:8	RG_VCAMAF_CAL	**Calibrates voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: 160mV 4'b1001: 140mV 4'b1010: 120mV 4'b1011: 100mV 4'b1100: 80mV 4'b1101: 60mV 4'b1110: 40mV 4'b1111: 20mV
6:4	RG_VCAMAF_VOSEL	**Selects output voltage** (3'b101: 2.8V) 3'b000: 1.2V 3'b001: 1.3V 3'b010: 1.5V 3'b011: 1.8V 3'b100: 2.0V 3'b101: 2.8V 3'b110: 3.0V 3'b111: 3.3V

0A6E **DLDO_ANA_CON2** **DLDO Control Register 2** **8050**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VIBR_NDIS_EN				RG_VIBR_CAL					RG_VIBR_VOSEL						
Type	RW				RW					RW						
Reset	1				0	0	0	0		1	0	1				

Bit(s)	Name	Description
15	RG_VIBR_NDIS_EN	**Enables power down NMOS** 1'b1: Enable 1'b0: Disable
11:8	RG_VIBR_CAL	**Calibrates voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV

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Bit(s)	Name	Description
		4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: 160mV 4'b1001: 140mV 4'b1010: 120mV 4'b1011: 100mV 4'b1100: 80mV 4'b1101: 60mV 4'b1110: 40mV 4'b1111: 20mV
6:4	RG_VIBR_VOSEL	**Selects output voltage** (3'b101: 2.8V) 3'b000: 1.2V 3'b001: 1.3V 3'b010: 1.5V 3'b011: 1.8V 3'b100: 2.0V 3'b101: 2.8V 3'b110: 3.0V 3'b111: 3.3V

0A70 **DLDO_ANA_CON3** **DLDO Control Register 3** **8000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VIO28_NDIS_EN				RG_VIO28_CAL											
Type	RW				RW											
Reset	1				0	0	0	0								

Bit(s)	Name	Description
15	RG_VIO28_NDIS_EN	**Enables power down NMOS** 1'b1: Enable 1'b0: Disable
11:8	RG_VIO28_CAL	**Calibrates voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: 160mV 4'b1001: 140mV 4'b1010: 120mV 4'b1011: 100mV 4'b1100: 80mV 4'b1101: 60mV 4'b1110: 40mV

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Bit(s)	Name	Description
		4'b1111: 20mV

0A72   DLDO_ANA_CON4   DLDO Control Register 4   8050

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VGP1_NDIS_EN				RG_VGP1_CAL					RG_VGP1_VOSEL						
Type	RW				RW					RW						
Reset	1				0	0	0	0		1	0	1				

Bit(s)	Name	Description
15	RG_VGP1_NDIS_EN	**Enables power down NMOS** 1'b1: Enable 1'b0: Disable
11:8	RG_VGP1_CAL	**Calibrates voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: 160mV 4'b1001: 140mV 4'b1010: 120mV 4'b1011: 100mV 4'b1100: 80mV 4'b1101: 60mV 4'b1110: 40mV 4'b1111: 20mV
6:4	RG_VGP1_VOSEL	**Selects output voltage** (3'b101: 2.8V) 3'b000: 1.2V 3'b001: 1.3V 3'b010: 1.5V 3'b011: 1.8V 3'b100: 2.5V 3'b101: 2.8V 3'b110: 3.0V 3'b111: 3.3V

0A74   DLDO_ANA_CON5   DLDO Control Register 5   0030

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_DLDO_RSV_H				RG_DLDO_RSV_L	
Type											RW				RW	

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Reset											1	1			0	0

Bit(s)	Name	Description
5:4	RG_DLDO_RSV_H	
1:0	RG_DLDO_RSV_L	

0A76 SLDO_ANA_CON0 SLDO Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**RG_VM_VOSEL**	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	RG_VM_VOSEL	**Selects output voltage** 2'b00: 1.24V 2'b01: 1.39V 2'b10: 1.54V

0A78 SLDO_ANA_CON1 SLDO Control Register 1 8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_VM_NDIS_EN**				**RG_VM_CAL**											
Type	RW				RW											
Reset	1				0	0	0	0								

Bit(s)	Name	Description
15	RG_VM_NDIS_EN	**Enables power down NMOS** 1'b1: Enable 1'b0: Disable
11:8	RG_VM_CAL	**Calibrates voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: 160mV 4'b1001: 140mV 4'b1010: 120mV 4'b1011: 100mV 4'b1100: 80mV 4'b1101: 60mV

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Bit(s)	Name	Description
		4'b1110: 40mV 4'b1111: 20mV

0A7A **SLDO_ANA_CON2** **SLDO Control Register 2** **8040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VCAMD_NDIS_EN				RG_VCAMD_CAL					RG_VCAMD_VOSEL						
Type	RW				RW					RW						
Reset	1				0	0	0	0		1	0	0				

Bit(s)	Name	Description
15	RG_VCAMD_NDIS_EN	**Enables power down NMOS** 1'b1: Enable 1'b0: Disable
11:8	RG_VCAMD_CAL	**Calibrates voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: 160mV 4'b1001: 140mV 4'b1010: 120mV 4'b1011: 100mV 4'b1100: 80mV 4'b1101: 60mV 4'b1110: 40mV 4'b1111: 20mV
6:4	RG_VCAMD_VOSEL	**Selects output voltage** (3'b100: 1.3V) 3'b000: 0.9V 3'b001: 1.0V 3'b010: 1.1V 3'b011: 1.22V 3'b100: 1.3V 3'b101: 1.5V

0A7C **SLDO_ANA_CON3** **SLDO Control Register 3** **8000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VRF18_0				RG_VRF18_0_CAL											

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	_NDIS_EN															
Type	RW				RW											
Reset	1				0	0	0	0								

Bit(s)	Name	Description
15	RG_VRF18_0_NDIS_EN	**Enables power down NMOS** 1'b1: Enable 1'b0: Disable
11:8	RG_VRF18_0_CAL	**Calibrates voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: 160mV 4'b1001: 140mV 4'b1010: 120mV 4'b1011: 100mV 4'b1100: 80mV 4'b1101: 60mV 4'b1110: 40mV 4'b1111: 20mV

0A7E **SLDO_ANA_CON4** **SLDO Control Register 4** **8030**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VRF18_1_NDIS_EN				RG_VRF18_1_CAL						RG_VRF18_1_VOSEL					
Type	RW				RW						RW					
Reset	1				0	0	0	0			1	1				

Bit(s)	Name	Description
15	RG_VRF18_1_NDIS_EN	**Enables power down NMOS** 1'b1: Enable 1'b0: Disable
11:8	RG_VRF18_1_CAL	**Calibrates voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: 160mV

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Bit(s)	Name	Description
		4'b1001: 140mV 4'b1010: 120mV 4'b1011: 100mV 4'b1100: 80mV 4'b1101: 60mV 4'b1110: 40mV 4'b1111: 20mV
5:4	RG_VRF18_1_VOSEL	**RG_VRF18_1_VOSEL[1:0]&RG_SLDO_RSV_L<2>** 2'b00 & RG_SLDO_RSV_L<2>=1: 1.2 v 2'b01 & RG_SLDO_RSV_L<2>=1: 1.3 v 2'b10 & RG_SLDO_RSV_L<2>=1: 1.5 v 2'b11 & RG_SLDO_RSV_L<2>=1: 1.8 v 2'b11 & RG_SLDO_RSV_L<2>=0: 1.825 v

0A80 SLDO_ANA_CON5 SLDO Control Register 5 8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VIO18_NDIS_EN				RG_VIO18_CAL											
Type	RW				RW											
Reset	1				0	0	0	0								

Bit(s)	Name	Description
15	RG_VIO18_NDIS_EN	**Enables power down NMOS** 1'b1: Enable 1'b0: Disable
11:8	RG_VIO18_CAL	**Calibrates voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: 160mV 4'b1001: 140mV 4'b1010: 120mV 4'b1011: 100mV 4'b1100: 80mV 4'b1101: 60mV 4'b1110: 40mV 4'b1111: 20mV

0A82 SLDO_ANA_CON6 SLDO Control Register 6 8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_				RG_VCN18_CAL											

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	VCN18_NDIS_EN															
Type	RW				RW											
Reset	1				0	0	0	0								

Bit(s)	Name	Description
15	RG_VCN18_NDIS_EN	**Enables power down NMOS** 1'b1: Enable 1'b0: Disable
11:8	RG_VCN18_CAL	**Calibrates voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: 160mV 4'b1001: 140mV 4'b1010: 120mV 4'b1011: 100mV 4'b1100: 80mV 4'b1101: 60mV 4'b1110: 40mV 4'b1111: 20mV

0A84 SLDO_ANA_CON7 SLDO Control Register 7 8030

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VCAMIO_NDIS_EN				RG_VCAMIO_CAL						RG_VCAMIO_VOSEL					
Type	RW				RW						RW					
Reset	1				0	0	0	0			1	1				

Bit(s)	Name	Description
15	RG_VCAMIO_NDIS_EN	**Enables power down NMOS** 1'b1: Enable 1'b0: Disable
11:8	RG_VCAMIO_CAL	**Calibrates voltage** (4'b0000: 0mV) 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV

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Bit(s)	Name	Description
		4'b0111: -140mV 4'b1000: 160mV 4'b1001: 140mV 4'b1010: 120mV 4'b1011: 100mV 4'b1100: 80mV 4'b1101: 60mV 4'b1110: 40mV 4'b1111: 20mV
5:4	RG_VCAMIO_VOSEL	**Selects output voltage** (2'b11: 1.8V) 2'b00: 1.2V 2'b01: 1.3V 2'b10: 1.5V 2'b11: 1.8V

0A86 SLDO_ANA_CON8 SLDO Control Register 8 0070

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_SLDO_RSV_H				RG_SLDO_RSV_L		
Type										RW				RW		
Reset										1	1	1		0	0	0

Bit(s)	Name	Description
6:4	RG_SLDO_RSV_H	
2:0	RG_SLDO_RSV_L	RG_SLDO_RSV_L[2] is used in conjunction with RG_VRF18_1_VOSEL[1:0].

0A88 SLDO_ANA_CON9 SLDO Control Register 9 0060

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_VSRAM_VOSEL						
Type										RW						
Reset										1	1	0	0	0	0	0

Bit(s)	Name	Description
6:0	RG_VSRAM_VOSEL	**Selects LDO voltage** (7'b0000000: 0.6V) 7'b0000000: 0.6V 7'b0000001: 0.6V + 6.25mV 7'b0000010: 0.6V + 6.25mV*2 7'b0000011: 0.6V + 6.25mV*3 7'b0000100: 0.6V + 6.25mV*4 7'b0000101: 0.6V + 6.25mV*5 7'b0000110: 0.6V + 6.25mV*6 7'b0000111: 0.6V + 6.25mV*7 7'b0001000: 0.6V + 6.25mV*8 7'b0001001: 0.6V + 6.25mV*9 7'b0001010: 0.6V + 6.25mV*10

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Bit(s)	Name	Description
		7'b0001011: 0.6V + 6.25mV*11
		7'b0001100: 0.6V + 6.25mV*12
		7'b0001101: 0.6V + 6.25mV*13
		7'b0001110: 0.6V + 6.25mV*14
		7'b0001111: 0.6V + 6.25mV*15
		7'b0010000: 0.6V + 6.25mV*16
		7'b0010001: 0.6V + 6.25mV*17
		7'b0010010: 0.6V + 6.25mV*18
		7'b0010011: 0.6V + 6.25mV*19
		7'b0010100: 0.6V + 6.25mV*20
		7'b0010101: 0.6V + 6.25mV*21
		7'b0010110: 0.6V + 6.25mV*22
		7'b0010111: 0.6V + 6.25mV23
		7'b0011000: 0.6V + 6.25mV*24
		7'b0011001: 0.6V + 6.25mV*25
		7'b0011010: 0.6V + 6.25mV*26
		7'b0011011: 0.6V + 6.25mV*27
		7'b0011100: 0.6V + 6.25mV*28
		7'b0011101: 0.6V + 6.25mV*29
		7'b0011110: 0.6V + 6.25mV*30
		7'b0011111: 0.6V + 6.25mV*31
		7'b0100000: 0.6V + 6.25mV*32
		7'b0100001: 0.6V + 6.25mV*33
		7'b0100010: 0.6V + 6.25mV*34
		7'b0100011: 0.6V + 6.25mV*35
		7'b0100100: 0.6V + 6.25mV*36
		7'b0100101: 0.6V + 6.25mV*37
		7'b0100110: 0.6V + 6.25mV*38
		7'b0100111: 0.6V + 6.25mV*39
		7'b0101000: 0.6V + 6.25mV*40
		7'b0101001: 0.6V + 6.25mV*41
		7'b0101010: 0.6V + 6.25mV*42
		7'b0101011: 0.6V + 6.25mV*45
		7'b0101100: 0.6V + 6.25mV*44
		7'b0101101: 0.6V + 6.25mV*45
		7'b0101110: 0.6V + 6.25mV*46
		7'b0101111: 0.6V + 6.25mV*47
		7'b0110000: 0.6V + 6.25mV*48
		7'b0110001: 0.6V + 6.25mV*49
		7'b0110010: 0.6V + 6.25mV*50
		7'b0110011: 0.6V + 6.25mV*51
		7'b0110100: 0.6V + 6.25mV*52
		7'b0110101: 0.6V + 6.25mV*53
		7'b0110110: 0.6V + 6.25mV*54
		7'b0110111: 0.6V + 6.25mV*55
		7'b0111000: 0.6V + 6.25mV*56
		7'b0111001: 0.6V + 6.25mV*57
		7'b0111010: 0.6V + 6.25mV*58
		7'b0111011: 0.6V + 6.25mV*59
		7'b0111100: 0.6V + 6.25mV*60
		7'b0111101: 0.6V + 6.25mV*61
		7'b0111110: 0.6V + 6.25mV*62
		7'b0111111: 0.6V + 6.25mV*63
		7'b1000000: 0.6V + 6.25mV*64
		7'b1000001: 0.6V + 6.25mV*65
		7'b1000010: 0.6V + 6.25mV*66
		7'b1000011: 0.6V + 6.25mV*67
		7'b1000100: 0.6V + 6.25mV*68
		7'b1000101: 0.6V + 6.25mV*69
		7'b1000110: 0.6V + 6.25mV*70
		7'b1000111: 0.6V + 6.25mV*71

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Bit(s)	Name	Description
		7'b1001000: 0.6V + 6.25mV*72
		7'b1001001: 0.6V + 6.25mV*73
		7'b1001010: 0.6V + 6.25mV*74
		7'b1001011: 0.6V + 6.25mV*75
		7'b1001100: 0.6V + 6.25mV*76
		7'b1001101: 0.6V + 6.25mV*77
		7'b1001110: 0.6V + 6.25mV*78
		7'b1001111: 0.6V + 6.25mV*79
		7'b1010000: 0.6V + 6.25mV*80
		7'b1010001: 0.6V + 6.25mV*81
		7'b1010010: 0.6V + 6.25mV*82
		7'b1010011: 0.6V + 6.25mV*93
		7'b1010100: 0.6V + 6.25mV*84
		7'b1010101: 0.6V + 6.25mV*85
		7'b1010110: 0.6V + 6.25mV*86
		7'b1010111: 0.6V + 6.25mV*87
		7'b1011000: 0.6V + 6.25mV*88
		7'b1011001: 0.6V + 6.25mV*89
		7'b1011010: 0.6V + 6.25mV*90
		7'b1011011: 0.6V + 6.25mV*91
		7'b1011100: 0.6V + 6.25mV*92
		7'b1011101: 0.6V + 6.25mV*93
		7'b1011110: 0.6V + 6.25mV*94
		7'b1011111: 0.6V + 6.25mV*95
		7'b1100000: 0.6V + 6.25mV*96
		7'b1100001: 0.6V + 6.25mV*97
		7'b1100010: 0.6V + 6.25mV*98
		7'b1100011: 0.6V + 6.25mV*99
		7'b1100100: 0.6V + 6.25mV*100
		7'b1100101: 0.6V + 6.25mV*101
		7'b1100110: 0.6V + 6.25mV*102
		7'b1100111: 0.6V + 6.25mV*103
		7'b1101000: 0.6V + 6.25mV*104
		7'b1101001: 0.6V + 6.25mV*105
		7'b1101010: 0.6V + 6.25mV*106
		7'b1101011: 0.6V + 6.25mV*107
		7'b1101100: 0.6V + 6.25mV*108
		7'b1101101: 0.6V + 6.25mV*109
		7'b1101110: 0.6V + 6.25mV*110
		7'b1101111: 0.6V + 6.25mV*111
		7'b1110000: 0.6V + 6.25mV*112
		7'b1110001: 0.6V + 6.25mV*113
		7'b1110010: 0.6V + 6.25mV*114
		7'b1110011: 0.6V + 6.25mV*115
		7'b1110100: 0.6V + 6.25mV*116
		7'b1110101: 0.6V + 6.25mV*117
		7'b1110110: 0.6V + 6.25mV*118
		7'b1110111: 0.6V + 6.25mV*119
		7'b1111000: 0.6V + 6.25mV*120
		7'b1111001: 0.6V + 6.25mV*121
		7'b1111010: 0.6V + 6.25mV*122
		7'b1111011: 0.6V + 6.25mV*123
		7'b1111100: 0.6V + 6.25mV*124
		7'b1111101: 0.6V + 6.25mV*125
		7'b1111110: 0.6V + 6.25mV*126
		7'b1111111: 0.6V + 6.25mV*127

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0A8A **SLDO_ANA_CON10** **SLDO Control Register10** **8000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VSRAM_NDIS_EN													RG_VSRAM_NDIS_PLCUR		RG_VSRAM_PLCUR_EN
Type	RW													RW		RW
Reset	1													0	0	0

Bit(s)	Name	Description
15	RG_VSRAM_NDIS_EN	**Enables LDO output power down NMOS discharge** 1'b0: Disable output power-down 1'b1: Enable output power-down
2:1	RG_VSRAM_NDIS_PLCUR	**Selects discharge current for DVFS tracking** (2'b00: 100mA) 2'b00: 100mA 2'b01: 130mA 2'b10: 130mA 2'b11: 160mA
0	RG_VSRAM_PLCUR_EN	**Improves VSRAM fast-transient** 0: Disable 1: Enable

0A90 **SPK_CON0** **Speaker Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_SPK_GAINL			SPK_OUT_STAGE_SEL	SPK_THER_SHDN_L_EN	SPK_OC_SHDN_DL					SPK_TRIM_EN_L	SPK MODE_L		SPK_EN_L
Type			RW			RW	RW	RW					RW	RW		RW
Reset			0	0		0	0	0					0	0		0

Bit(s)	Name	Description
13:12	RG_SPK_GAINL	**Controls speaker L-ch volume** 2'b00: Mute 2'b01: -6dB 2'b10: -3dB 2'b11: 0dB
10	SPK_OUT_STAGE_SEL	**Selects OUTSTAGE after trimming enabled** 1'b0: Disable 1'b1: Enable
9	SPK_THER_SHDN_L_EN	**Enables speaker L-ch thermal shut-down** 1'b0: Disable 1'b1: Enable
8	SPK_OC_SHDN_DL	**Class D mode L-ch OC event shut-down** 1'b0: Normal 1'b1: Shut down (turn off SPK output stage)
3	SPK_TRIM_EN_L	**Enables class D mode L-ch trimming**

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Bit(s)	Name	Description
		1'b0: Disable 1'b1: Enable
2	SPKMODE_L	**Selects speaker L-ch driver mode** 1'b0: Class D mode 1'b1: Class AB mode
0	SPK_EN_L	**Enables speaker amp. L-ch** 1'b0: Disable 1'b1: Enable

0A92 SPK_CON1 Speaker Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPK_TRIM_DONE_L	SPK_OFFSET_L_MODE	SPK_LEAD_L_SW	SPK_OFFSET_L_SW					SPK_OFFSET_L_OV							
Type	RO	RW	RW	RW					RO							
Reset	0	0	0	0	0	0	0	0	0							

Bit(s)	Name	Description
15	SPK_TRIM_DONE_L	**Class D mode L-ch trimming done** 1'b0: Not yet 1'b1: Done
14	SPK_OFFSET_L_MODE	**Selects SPK_OFFSET_L mode** 1'b0: Calibration 1'b1: Software register mode
13	SPK_LEAD_L_SW	**Class D L-ch PWM polarity flag**
12:8	SPK_OFFSET_L_SW	**Speaker amplifier left channel offset trimming bit** 5'b00000: 0mV 5'b00001: 0.6mV 5'b00010: 1.2mV xxx: xxxV (omit) 5'b11111: 18.6mV
7	SPK_OFFSET_L_OV	**SPK_OFFSET_L overflow**

0A94 SPK_CON2 Speaker Control Register 2 0014

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_SPK_OC_EN_L	RG_SPKAB_OC_EN_L	RG_SPK_TEST_EN_L	RG_SPK_DRC_EN_L	RG_SPKRCV_EN_L	RG_SPKAB_OBIAS_L		RG_SPK_SLEW_L		RG_SPK_FORCE_EN_L	RG_SPK_INTG_RST_L
Type						RW	RW	RW	RW	RW	RW		RW		RW	RW
Reset						0	0	0	0	0	0	1	0	1	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
10	RG_SPK_OC_EN_L	**Enables class D L-ch over-current protection** 1'b0: Disable 1'b1: Enable
9	RG_SPKAB_OC_EN_L	**Enables class AB mode L-ch Over-current protection**
8	RG_SPK_TEST_EN_L	**Enables test input into SPK stage** (Not used)
7	RG_SPK_DRC_EN_L	**Reserved** (Not used)
6	RG_SPKRCV_EN_L	**Reserved** 1'b0: Disable 1'b1: Enable
5:4	RG_SPKAB_OBIAS_L	**Controls L-ch classAB SPK bias** 00: 2I 11: 8I step=2I
3:2	RG_SPK_SLEW_L	**Controls class D L-ch slew rate** 00: 3/4 (default)10.8n /8.3n (rise/fall) 01: 4/4 8.8n /6.3n 10: 1/4 16.4n /15n 11: 2/4 3.8n/12.6n
1	RG_SPK_FORCE_EN_L	**Forces L-ch class D output state** 1'b0: Disable 1'b1: Enable
0	RG_SPK_INTG_RST_L	**Controls speaker L-ch integrator reset** 1'b0: No reset 1'b1: Reset on

0A9C **SPK_CON6** **Speaker Control Register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPK_AB_OC_L_DEG	SPK_D_OC_L_DEG			SPK_OC_THD		SPK_OC_WND				SPK_TRIM_THD			SPK_TRIM_WND		
Type	RO	RO			RW		RW				RW			RW		
Reset	0	0			0	0	0	0			0	0		0	0	0

Bit(s)	Name	Description
15	SPK_AB_OC_L_DEG	**Class AB L-ch OC flag with deglitch**
14	SPK_D_OC_L_DEG	**Class D L-ch OC flag with deglitch**
11:10	SPK_OC_THD	**Threshold setting in the decision window for SPK over current status** 2'b00: 4/8 2'b01: 3/8 2'b10: 2/8 2'b11: 1/8
9:8	SPK_OC_WND	**Decision window setting for SPK over current status** 2'b00: 16us 2'b01: 32us 2'b10: 64us

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Bit(s)	Name	Description
		2'b11: 128us
5:4	SPK_TRIM_THD	**Threshold setting in the decision window for SPK offset status** 2'b00: 4/8 2'b01: 3/8 2'b10: 2/8 2'b11: 1/8
2:0	SPK_TRIM_WND	**Decision window setting for SPK offset status** 3'b000: 16us 3'b001: 32us 3'b010: 64us 3'b011: 128us 3'b100: 256us 3'b101: 512us 3'b110: 1024us 3'b111: 2048us

0A9E **SPK_CON7** **Speaker Control Register 7** **4531**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		SPK_TRIM_DIV			SPK_TD3				SPK_TD2				SPK_TD1			
Type		RW			RW				RW				RW			
Reset		1	0	0	0	1	0	1	0	0	1	1	0	0	0	1

Bit(s)	Name	Description
14:12	SPK_TRIM_DIV	**Divider of AD_NI_SPK_CK_PWM for trimming counter clock** 3'b000: 8 3'b001: 16 3'b010: 32 3'b011: 64 3'b100: 128 3'b101: 256 3'b110: 512 3'b111: 1024
11:8	SPK_TD3	**Time delay3 for TRIM_EN** 4'd0: 0ms 4'd1: 1ms 4'd2: 2ms 4'dN: nms 4'd15: 15ms
7:4	SPK_TD2	**Time delay2 for OUTSTG_EN** 4'd0: 0ms 4'd1: 1ms 4'd2: 2ms 4'dN: nms 4'd15: 15ms
3:0	SPK_TD1	**Time delay1 for VCM_FAST** 4'd0: 0ms 4'd1: 1ms 4'd2: 2ms 4'dN: nms 4'd15: 15ms

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0AA0 SPK_CON8 Speaker Control Register 8 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_SPK_OCTH_D	RG_SPKAB_OVDRV	RG_SPK_FBRC_EN	RG_SPK_VCM_IBSEL	RG_SPK_VCM_SEL	RG_SPK_EN_VIEW_CLK	RG_SPK_EN_VIEW_VCM	RG_SPK_CCODE				RG_SPK_IBIAS_SEL		RG_BTL_SET	
Type		RW	RW	RW	RW	RW	RW	RW	RW				RW		RW	
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14	RG_SPK_OCTH_D	**Speaker OC threshold level for D-mode** 1'b0: Low (0.9A) 1'b1: High (1.5A)
13	RG_SPKAB_OVDRV	**Output stage shoot-through current prevention in over-drive condition of class AB mode** 1'b0: Disable 1'b1: Enable
12	RG_SPK_FBRC_EN	**Feedback grounded capacitor connection in class D state** 1'b0: Disable 1'b1: Enable
11	RG_SPK_VCM_IBSEL	**Selects speaker on-chip filter bias current level** 1'b0: Normal bias (low BW) 1'b1: Doubled bias (high BW)
10	RG_SPK_VCM_SEL	**Selects speaker VCM source** 1'b0: 0.5*AVDD43 1'b1: IR, I from BG
9	RG_SPK_EN_VIEW_CLK	**Enables monitor class D PWM CLK**
8	RG_SPK_EN_VIEW_VCM	**Enables monitor speaker VCM reference voltage**
7:4	RG_SPK_CCODE	**Class D modulation frequency control code** x000: 288k x001: 418.8k x010: 541k x011: 656k x100: 766k x101: 966k x110: 1.148M x111: 1.646M
3:2	RG_SPK_IBIAS_SEL	**Controls internal bias current generator** 2'b00: Default 2'b01: -20% 2'b10: +20% 2'b11: +10%
1:0	RG_BTL_SET	**Sets up class D BTL output when RG_FORCE_EN=1** <1> 1: SPK+ NMOS on; 0: SPK+ PMOS on <0> 1: SPK- NMOS on; 0: SPK- PMOS on

0AA2 SPK_CON9 Speaker Control Register 9 2000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	SPK_TEST_MODE1	SPK_TEST_MODE0	SPK_VCM_FAST_EN	SPK_RSV0	RG_SPKPGA_GAINL											
Type	RW	RW	RW	RW	RW											
Reset	0	0	1	0	0	0	0	0								

Bit(s)	Name	Description
15	SPK_TEST_MODE1	**SPK testmode 1**
14	SPK_TEST_MODE0	**SPK testmode 0**
13	SPK_VCM_FAST_EN	**Enables QI_SPK_VCM_FAST in hardware mode**
12	SPK_RSV0	
11:8	RG_SPKPGA_GAINL	**Controls speaker L PGA gain** 4'b0000: Mute 4'b0001: 0dB 4'b0010: 4dB 4'b0011: 5dB 4'b0100: 6dB 4'b0101: 7dB 4'b0110: 8dB 4'b0111: 9dB 4'b1000: 10dB 4'b1001: 11dB 4'b1010: 12dB 4'b1011: 13dB 4'b1100: 14dB 4'b1101: 15dB 4'b1110: 16dB 4'b1111: 17dB

0AA4 SPK_CON10 Speaker Control Register 10 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										SPK_TD_DONE				SPK_TD_WAIT		
Type										RW				RW		
Reset										0	0	0		0	0	0

Bit(s)	Name	Description
6:4	SPK_TD_DONE	**Done time** 3'b000: 10us 3'b001: 50us 3'b010: 100us 3'b011: 300us 3'b100: 500us 3'b101: 1000us 3'b110: 1500us 3'b111: 2000us
2:0	SPK_TD_WAIT	**Wait time** 3'b000: 10us 3'b001: 50us 3'b010: 100us 3'b011: 300us 3'b100: 500us 3'b101: 1000us

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Bit(s)	Name	Description
		3'b110: 1500us 3'b111: 2000us

0AA6 **SPK_CON11** **Speaker Control Register 11** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPK_TRIM_STOP_L_SW		SPK_TRIM_EN_L_SW		SPK_OUTSTG_EN_L_SW		SPK_EN_L_SW		SPK_DEPOP_EN_L_SW		SPKMODE_L_SW		SPK_RST_L_SW		SPK_VCM_FAST_SW	SPK_EN_MODE
Type	RW		RW		RW		RW		RW		RW		RW		RW	RW
Reset	0		0		0		0		0		0		0		0	0

Bit(s)	Name	Description
15	SPK_TRIM_STOP_L_SW	**Class D mode offset trimming stop flag for L-ch**
13	SPK_TRIM_EN_L_SW	**Class D mode L-ch offset trimming start flag**
11	SPK_OUTSTG_EN_L_SW	**Speaker left channel output stage enable control**
9	SPK_EN_L_SW	**Enables speaker amp. L-ch** 1'b0: Disable 1'b1: Enable
7	SPK_DEPOP_EN_L_SW	**Class D L-ch mode depop enabled flag**
5	SPKMODE_L_SW	**Selects speaker L-ch driver mode** 1'b0: Class D mode 1'b1: Class AB mode
3	SPK_RST_L_SW	**Resets class D L-ch** 1'b0: Normal 1'b1: Reset
1	SPK_VCM_FAST_SW	**Speeds up speaker VCM settling when enabled** 1'b0: Normal 1'b1: Fast charging
0	SPK_EN_MODE	**Selects speaker enable sequence** 1'b0: HW 1'b1: SW (register mode)

0AA8 **SPK_CON12** **Speaker Control Register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SPK_ISENSE_EN	RG_SPK_ISENSE_PDRESET	RG_SPK_ISENSE_GAINSEL			RG_SPK_ISENSE_REFSEL			RG_SPK_ISENSE_TEST_EN							
Type	RW	RW	RW			RW			RW							
Reset	0	0	0	0	0	0	0	0	0							

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Bit(s)	Name	Description
15	RG_SPK_ISENSE_EN	**Enables class AB current sensing circuit** 1'b0: Disable 1'b1: Enable
14	RG_SPK_ISENSE_PDRESET	**Resets class AB current sensing peak detection** 1'b0: Disable 1'b1: Enable
13:11	RG_SPK_ISENSE_GAINSEL	**Selects class AB current sensing circuit gain** 3'b000: 0dB 3'b001: 6dB 3'b010: 12dB 3'b011: 18dB 3'b100: 24dB 3'b101: 30dB 3'b110~3'b111: Reserved
10:8	RG_SPK_ISENSE_REFSEL	**selects class AB current sensing circuit reference** 3'b000: AVSS43_SPK 3'b001: NMOS gate voltage @40uA 3'b010: NMOS gate voltage @80uA 3'b011: NMOS gate voltage @120uA 3'b100: NMOS gate voltage @160uA 3'b101: NMOS gate voltage @200uA 3'b110: NMOS gate voltage @240uA 3'b111: NMOS gate voltage @280uA
7	RG_SPK_ISENSE_TEST_EN	**(Not used)** 1'b0: Disable 1'b1: Enable

0AAA SPK_CON13 Speaker Control Register 13 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SPK_RSV0								RG_SPK_RSV1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	RG_SPK_RSV0	**[15:14]: Not used** [13]: Enable Class-AB CLP [12:11]: Additional control on offset trimming circuit 2'b00: Normal operation (triangle modulation waveform) 2'b11: Trimming operation (sawtooth modulation waveform) [10]: RG_TRIM_INV 1'b1: Inverting phase 1'b0: Default phase [9]: Enable Class-AB DFC (EN_AB_DFC) [8]: Enable PGA DLCK (EN_PGA_DLCK)
7:0	RG_SPK_RSV1	**(Not used)**

0AAC SPK_CON14 Speaker Control Register 14 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	RG_SPK_RSV2								RG_SPK_ABD_CURSEN_SEL	RG_SPK_ABD_VOLSEN_EN	RG_SPK_ABD_VOLSEN_GAIN					
Type	RW								RW	RW	RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
15:8	RG_SPK_RSV2	**(Not used)**
7	RG_SPK_ABD_CURSEN_SEL	**(Not used)**
6	RG_SPK_ABD_VOLSEN_EN	**Controls class ABD voltage sensing** 1'b0: Disable 1'b1: Enable
5:4	RG_SPK_ABD_VOLSEN_GAIN	**Controls class ABD voltage sensing gain** 2'b00: -6dB 2'bx1: -18dB 2'b10: -12dB

0AAE <u>SPK_CON15</u> Speaker Control Register 15 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SPK_TRIM1								RG_SPK_TRIM2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	RG_SPK_TRIM1	(Not used)
7:0	RG_SPK_TRIM2	(Not used)

0AB0 <u>SPK_CON16</u> Speaker Control Register 16 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_SPK_AB_CURSEN_EN	RG_SPK_AB_CURSEN_GAIN		RG_SPK_AB_CURSEN_RSETSEL					RG_SPK_D_CURSEN_EN	RG_SPK_D_CURSEN_GAIN		RG_SPK_D_CURSEN_RSETSEL				
Type	RW	RW		RW					RW	RW		RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RG_SPK_AB_CURSEN_EN	**Controls class AB current sensing** 1'b0: Disable 1'b1: Enable
14:13	RG_SPK_AB_CURSEN_GAIN	**Controls class AB current sensing grain** 2'b00: -6dB 2'bx1: -18dB

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Bit(s)	Name	Description
		2'b10: -12dB
12:8	RG_SPK_AB_CURSEN_RSETSEL	**(Not used)**
7	RG_SPK_D_CURSEN_EN	**(Not used)**
6:5	RG_SPK_D_CURSEN_GAIN	**(Not used)**
4:0	RG_SPK_D_CURSEN_RSETSEL	**(Not used)**

0AB2 **SPK_ANA_CON0** **SPK Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**RG_SPKPGA_GAIN**														
Type		RW														
Reset		0	0	0	0											

Bit(s)	Name	Description
14:11	RG_SPKPGA_GAIN	**Controls speaker PGA gain** 0000: Mute 0001: 0dB 0010: 4dB 0011: 5dB 0100: 6dB 0101: 7dB 0110: 8dB 0111: 9dB 1000: 10dB 1001: 11dB 1010: 12dB 1011: 13dB 1100: 14dB 1101: 15dB 1110: 16dB 1111: 17dB

0AB4 **SPK_ANA_CON1** **SPK Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RG_ISENSE_PD_RESET**				**RG_SPK_RSV**							
Type					RW				RW							
Reset					0				0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	RG_ISENSE_PD_R	**Resets class AB current sensing peak detector**

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Bit(s)	Name	Description
	ESET	0: Disable 1: Enable
7:0	RG_SPK_RSV	**Reserved**

0AB6 **SPK_ANA_CON3** **SPK Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_AUDIVLMUTE_VAUDP12	RG_AUDIVLMUXSEL_VAUDP12			RG_AUDIVLSTARTUP_VAUDP12	RG_AUDIVLPWRUP_VAUDP12				
Type							RW	RW			RW	RW				
Reset							0	0	0	0	0	0				

Bit(s)	Name	Description
9	RG_AUDIVLMUTE_VAUDP12	**Enables audio left channel I-V buffer mute**
8:6	RG_AUDIVLMUXSEL_VAUDP12	**Selects audio left channel IV buffer mux** Positive/negative pins: 000: Open/Open 001: FM stereo mode 010: FM mono mode 011: Open/Open 100: Audio playback mode 101: Audio + FM stereo mode 110: Audio + FM mono mode 111: Audio playback mode
5	RG_AUDIVLSTARTUP_VAUDP12	**Enables audio left channel I-V buffer startup**
4	RG_AUDIVLPWRUP_VAUDP12	**Powers up audio left channel I-V buffer**

0C00 **OTP_CON0** **OTP Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_OTP_PA					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	RG_OTP_PA	OTP PA

0C02 **OTP_CON1** **OTP Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name									**RG_OTP_PDIN**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RG_OTP_PDIN	OTP PDIN

0C04 OTP_CON2 OTP Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**RG_OTP_PTM**	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	RG_OTP_PTM	OTP PTM

0C06 OTP_CON3 OTP Control Register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**RG_OTP_PWE**	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	RG_OTP_PWE	OTP PWE

0C08 OTP_CON4 OTP Control Register 4 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RG_OTP_PPROG**
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_OTP_PPROG	OTP PPROG

0C0A OTP_CON5 OTP Control Register 5 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RG_OTP_PWE_S**

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																RC
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_OTP_PWE_SRC	**Selects OTP write (fusing) PWE source** 0: From IO pad 1: From register

0C0C OTP_CON6 OTP Control Register 6 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_OTP_PROG_PKEY**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_PROG_PKEY	OTP write (fusing) match key

0C0E OTP_CON7 OTP Control Register 7 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_OTP_RD_PKEY**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_RD_PKEY	OTP read match key

0C10 OTP_CON8 OTP Control Register 8 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**RG_OTP_RD_TRIG**
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_OTP_RD_TRIG	OTP SW read trigger

0C12 OTP_CON9 OTP Control Register 9 0000

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_RD_RDY_BYPASS
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_RD_RDY_BYPASS	**Bypasses OTP read ready delay** 0: Does not bypass 1: Bypass

0C14 OTP_CON10 OTP Control Register 10 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_SKIP_OTP_OUT
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_SKIP_OTP_OUT	**Skips reading from EFUSE macro** 0: Does not skip 1: Skip

0C16 OTP_CON11 OTP Control Register 11 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_OTP_RD_SW
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_OTP_RD_SW	**SW trigger read mode** 0: Not SW trigger read mode 1: SW trigger read mode

0C18 OTP_CON12 OTP Control Register 12 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_SW															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	RG_OTP_DOUT_SW	Current SW trigger read value

0C1A **OTP_CON13** **OTP Control Register 13** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_OTP_RD_ACK		RG_OTP_RD_BUSY
Type														RO		RO
Reset														0		0

Bit(s)	Name	Description
2	RG_OTP_RD_ACK	OTP read ack
0	RG_OTP_RD_BUSY	OTP busy status

0C1C **OTP_CON14** **OTP Control Register 14** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_OTP_PA_SW				
Type												RO				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RG_OTP_PA_SW	Current SW trigger read row

0C1E **OTP_DOUT_0_15** **OTP dout 0 15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_0_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_0_15	

0C20 **OTP_DOUT_16_31** **OTP dout 16 31** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_16_31															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_16_31	

0C22 **OTP_DOUT_32_47** **OTP dout 32 47** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_OTP_DOUT_32_47**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_32_47	

0C24 **OTP_DOUT_48_63** **OTP dout 48 63** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_OTP_DOUT_48_63**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_48_63	

0C26 **OTP_DOUT_64_79** **OTP dout 64 79** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_OTP_DOUT_64_79**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_64_79	

0C28 **OTP_DOUT_80_95** **OTP dout 80 95** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	RG_OTP_DOUT_80_95															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_80_95	

0C2A **OTP_DOUT_96_111** **OTP dout 96 111** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_96_111															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_96_111	

0C2C **OTP_DOUT_112_127** **OTP dout 112 127** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_112_127															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_112_127	

0C2E **OTP_DOUT_128_143** **OTP dout 128 143** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_128_143															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_128_143	

0C30 **OTP_DOUT_144_159** **OTP dout 144 159** **0000**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_144_159															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_144_159	

0C32 **OTP_DOUT_160_175** **OTP dout 160 175** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_160_175															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_160_175	

0C34 **OTP_DOUT_176_191** **OTP dout 176 191** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_176_191															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_176_191	

0C36 **OTP_DOUT_192_207** **OTP dout 192 207** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_192_207															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_192_207	

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0C38 **OTP_DOUT_208_223** **OTP dout 208 223** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_208_223															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_208_223	

0C3A **OTP_DOUT_224_239** **OTP dout 224 239** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_224_239															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_224_239	

0C3C **OTP_DOUT_240_255** **OTP dout 240 255** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_240_255															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_240_255	

0C3E **OTP_DOUT_256_271** **OTP dout 256 271** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_256_271															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_256_271	

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0C40 **OTP_DOUT_272_287** **OTP dout 272 287** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_272_287															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_272_287	

0C42 **OTP_DOUT_288_303** **OTP dout 288 303** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_288_303															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_288_303	

0C44 **OTP_DOUT_304_319** **OTP dout 304 319** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_304_319															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_304_319	

0C46 **OTP_DOUT_320_335** **OTP dout 320 335** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_320_335															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_320_335	

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0C48 OTP_DOUT_336_351 OTP dout 336 351 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_336_351															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_336_351	

0C4A OTP_DOUT_352_367 OTP dout 352 367 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_352_367															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_352_367	

0C4C OTP_DOUT_368_383 OTP dout 368 383 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_368_383															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_368_383	

0C4E OTP_DOUT_384_399 OTP dout 384 399 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_384_399															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_384_399	

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0C50 **OTP_DOUT_400_415** **OTP dout 400 415** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_400_415															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_400_415	

0C52 **OTP_DOUT_416_431** **OTP dout 416 431** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_416_431															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_416_431	

0C54 **OTP_DOUT_432_447** **OTP dout 432 447** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_432_447															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_432_447	

0C56 **OTP_DOUT_448_463** **OTP dout 448 463** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_448_463															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_448_463	

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0C58 OTP_DOUT_464_479 OTP dout 464 479 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_464_479															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_464_479	

0C5A OTP_DOUT_480_495 OTP dout 480 495 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_480_495															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_480_495	

0C5C OTP_DOUT_496_511 OTP dout 496 511 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_DOUT_496_511															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_DOUT_496_511	

0C5E OTP_VAL_0_15 OTP val 0 15 0048

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_0_15															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_0_15	

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0C60 **OTP_VAL_16_31** **OTP val 16 31** **00B0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_16_31															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_16_31	

0C62 **OTP_VAL_32_47** **OTP val 32 47** **0160**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_32_47															
Type	RW															
Reset	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_32_47	

0C64 **OTP_VAL_48_63** **OTP val 48 63** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_48_63															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_48_63	

0C66 **OTP_VAL_64_79** **OTP val 64 79** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_64_79															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_64_79	

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0C68	OTP_VAL_80_95	OTP val 80 95	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_80_95															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_80_95	

0C6A	OTP_VAL_96_111	OTP val 96 111	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_96_111															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_96_111	

0C6C	OTP_VAL_112_127	OTP val 112 127	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_112_127															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_112_127	

0C6E	OTP_VAL_128_143	OTP val 128 143	000C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_128_143															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_128_143	

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0C70 **OTP_VAL_144_159** OTP val 144 159 **D000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_144_159															
Type	RW															
Reset	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_144_159	

0C72 **OTP_VAL_160_175** OTP val 160 175 **8000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_160_175															
Type	RW															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_160_175	

0C74 **OTP_VAL_176_191** OTP val 176 191 **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_176_191															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	RG_OTP_VAL_176_191	

0C76 **OTP_VAL_192_207** OTP val 192 207 **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_192_207															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_192_207	

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0C78 **OTP_VAL_208_223** **OTP val 208 223** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_208_223															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_208_223	

0C7A **OTP_VAL_224_239** **OTP val 224 239** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_224_239															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_224_239	

0C7C **OTP_VAL_240_255** **OTP val 240 255** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_240_255															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_240_255	

0C7E **OTP_VAL_256_271** **OTP val 256 271** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_256_271															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_256_271	

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0C80	OTP_VAL_272_287	OTP val 272 287	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_272_287															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_272_287	

0C82	OTP_VAL_288_303	OTP val 288 303	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_288_303															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_288_303	

0C84	OTP_VAL_304_319	OTP val 304 319	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_304_319															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_304_319	

0C86	OTP_VAL_320_335	OTP val 320 335	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_320_335															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_320_335	

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0C88 **OTP_VAL_336_351** **OTP val 336 351** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_336_351															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_336_351	

0C8A **OTP_VAL_352_367** **OTP val 352 367** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_352_367															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_352_367	

0C8C **OTP_VAL_368_383** **OTP val 368 383** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_368_383															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_368_383	

0C8E **OTP_VAL_384_399** **OTP val 384 399** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_384_399															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_384_399	

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0C90 **OTP_VAL_400_415** **OTP val 400 415** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_400_415															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_400_415	

0C92 **OTP_VAL_416_431** **OTP val 416 431** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_416_431															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_416_431	

0C94 **OTP_VAL_432_447** **OTP val 432 447** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_432_447															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_432_447	

0C96 **OTP_VAL_448_463** **OTP val 448 463** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_448_463															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_448_463	

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0C98 OTP_VAL_464_479 OTP val 464 479 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_464_479															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_464_479	

0C9A OTP_VAL_480_495 OTP val 480 495 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_480_495															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_480_495	

0C9C OTP_VAL_496_511 OTP val 496 511 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OTP_VAL_496_511															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_OTP_VAL_496_511	

0CA6 FGADC_CON1 FGADC Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_CAR_31_16															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_CAR_31_16	Current charge value[31:16]

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0CA8 FGADC_CON2 FGADC Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_CAR_15_00															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_CAR_15_00	Current charge value[15:0]

0CAA FGADC_CON3 FGADC Control Register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			FG_NTER_29_16													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	FG_NTER_29_16	Current charge time value[29:16]

0CAC FGADC_CON4 FGADC Control Register 4 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_NTER_15_00															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_NTER_15_00	Current charge time value[15:0]

0CB2 FGADC_CON7 FGADC Control Register 7 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FG_CURRENT_OUT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FG_CURRENT_OUT	Current output charge of first stage[15:0]

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0CB8 **FGADC_CON10** **FGADC Control Register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_SPARE								RG_FGINTMODE	RG_FGANALOGTEST			
Type				RW								RW	RW			
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:5	RG_SPARE	**Reserved bits**
4	RG_FGINTMODE	0: Battery bottom mode 1: Battery top mode
3:0	RG_FGANALOGTEST	**FGADC test bits**

0CDC **AUDDEC_ANA_CON0** **AUDDEC Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDHPRSCDISABLE_VAUDP15	RG_AUDHPLSCDISABLE_VAUDP15	RG_AUDHSSCDISABLE_VAUDP15	RG_AUDHPRMUXINPUTSEL_VAUDP15		RG_AUDHPLMUXINPUTSEL_VAUDP15		RG_AUDHSMUXINPUTSEL_VAUDP15		RG_AUDHPRPWRUP_VAUDP15	RG_AUDHPLPWRUP_VAUDP15	RG_AUDHSPWRUP_VAUDP15	RG_AUD_DAC_PWL_UP_VA28	RG_AUD_DAC_PWR_UP_VA28	RG_AUDDACRPWRUP_VAUDP15	RG_AUDDACLPWRUP_VAUDP15
Type	RW	RW	RW	RW		RW		RW		RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RG_AUDHPRSCDISABLE_VAUDP15	**Disables headphone right short circuit protection**
14	RG_AUDHPLSCDISABLE_VAUDP15	**Disables headphone left short circuit protection**
13	RG_AUDHSSCDISABLE_VAUDP15	**Disables headset short circuit protection**
12:11	RG_AUDHPRMUXINPUTSEL_VAUDP15	**Selects audio right headphone input multiplexer** Positive/negative pins: 00: Open/Open 01: LoudSPK playback 10: Audio playback 11: Test mode
10:9	RG_AUDHPLMUXINPUTSEL_VAUDP15	**Selects audio left headphone input multiplexer** Positive/negative pins: 00: Open/Open 01: LoudSPK playback 10: Audio playback 11: Test mode
8:7	RG_AUDHSMUXINPUTSEL_VAUDP15	**Selects audio handset input multiplexer Positive/negative pins:** 00: Open/Open 01: Mute (input grounded)

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Bit(s)	Name	Description
		10: Voice playback 11: Test mode
6	RG_AUDHPRPWRUP_VAUDP15	**Powers up audio right headphone**
5	RG_AUDHPLPWRUP_VAUDP15	**Powers up audio left headphone**
4	RG_AUDHSPWRUP_VAUDP15	**Powers up audio headset**
3	RG_AUD_DAC_PWL_UP_VA28	**Controls power-down for left channel audio biasgen** 0: Power down 1: Enable
2	RG_AUD_DAC_PWR_UP_VA28	**Controls power-down for right channel audio biasgen** 0: Power down 1: Enable
1	RG_AUDDACRPWRUP_VAUDP15	**Controls power-down for right-channel audio DAC** 0: Power down 1: Enable
0	RG_AUDDACLPWRUP_VAUDP15	**Controls power-down for left-channel audio DAC** 0: Power down 1: Enable

0CDE **AUDDEC_ANA_CON1** **AUDDEC Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_HSOUTPUTRESET0_VAUDP15	RG_HSINPUTRESET0_VAUDP15	RG_HSOUTPUTSTBENH_VAUDP15	RG_HSINPUTSTBENH_VAUDP15	RG_HPOUT_SHORTVCM_VAUDP15	RG_HPOUTPUTRESET0_VAUDP15	RG_HPINPUTRESET0_VAUDP15	RG_HPOUTPUTSTBENH_VAUDP15	RG_HPINPUTSTBENH_VAUDP15	RG_PRECHARGEBUF_EN_VAUDP15	RG_AUDHSSTARTUP_VAUDP15	RG_AUDHPSTARTUP_VAUDP15	RG_AUDHSBSCCURRENT_VAUDP15	RG_AUDHPRBSCCURRENT_VAUDP15	RG_AUDHPLBSCCURRENT_VAUDP15
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14	RG_HSOUTPUTRESET0_VAUDP15	**Resets HS driver DE outputs to 0V ground** 0: Does not reset 1: Reset
13	RG_HSINPUTRESET0_VAUDP15	**Resets HS driver DE inputs to 0V ground** 0: Does not reset 1: Reset
12	RG_HSOUTPUTSTBENH_VAUDP15	**HS driver output stability enhancement option** 0: No enhancement 1: Enhance
11	RG_HSINPUTSTBENH_VAUDP15	**HS driver input stability enhancement option** 0: No enhancement 1: Enhance
10	RG_HPOUT_SHORTVCM_VAUDP15	**Shorts HP output to VCM (DCC: 0V; ACC: 1.4V)** 0: Does not short to VCM

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Bit(s)	Name	Description
		1: Short to VCM
9	RG_HPOUTPUTRESET0_VAUDP15	**Resets HPL/R driver SE output to 0V ground** 0: Does not reset 1: Reset
8	RG_HPINPUTRESET0_VAUDP15	**Resets HP driver input to ground** 0: Does not reset 1: Reset
7	RG_HPOUTPUTSTBENH_VAUDP15	**HP driver output stability enhancement option** 0: No enhancement 1: Enhance
6	RG_HPINPUTSTBENH_VAUDP15	**HP driver input stability enhancement option** 0: No enhancement 1: Enhance
5	RG_PRECHARGEBUF_EN_VAUDP15	**Enables pre-charge buffer stage 2** 0: Disable 1: Enable
4	RG_AUDHSSTARTUP_VAUDP15	**Forces Startup mode in HS Amp if required**
3	RG_AUDHPSTARTUP_VAUDP15	**Forces Startup mode in HP Amps if required**
2	RG_AUDHSBSCCURRENT_VAUDP15	**Audio handset BSC current**
1	RG_AUDHPRBSCCURRENT_VAUDP15	**Audio right headphone BSC current**
0	RG_AUDHPLBSCCURRENT_VAUDP15	**Audio left headphone BSC current**

0CE0 **AUDDEC_ANA_CON2** **AUDDEC Control Register 2** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDHPRFINETRIM_VAUDP15		RG_AUDHPLFINETRIM_VAUDP15		RG_AUDHPTRIM_EN_VAUDP15	RG_AUDHPRTRIM_VAUDP15				RG_AUDHPLTRIM_VAUDP15				RG_HSOUT_SHORTVCM_VAUDP15	RG_HPOUTSTB_RSEL_VAUDP15	
Type	RW		RW		RW	RW				RW				RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:14	RG_AUDHPRFINETRIM_VAUDP15	**Fine trims offset voltage of HPR** 01: -0.5mV 10: +0.5mV
13:12	RG_AUDHPLFINETRIM_VAUDP15	**Fine trims offset voltage of HPL** 01: -0.5mV 10: +0.5mV
11	RG_AUDHPTRIM_EN_VAUDP15	**Enable control of trimming circuit of HP** 0: Disable trimming circuit 1: Enable trimming circuit

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Bit(s)	Name	Description
10:7	RG_AUDHPRTRIM_VAUDP15	**Trims offset voltage of HPR** 0000: 0V 0001: -0.5mV 0010: -1.5mV 0011: -2.5mV 0100: -3.5mV 0101: -4.5mV 0110: -5.5mV 0111: -6.5mV 1001: 0.5mV 1010: 1.5mV 1011: 2.5mV 1100: 3.5mV 1101: 4.5mV 1110: 5.5mV 1111: 6.5mV
6:3	RG_AUDHPLTRIM_VAUDP15	**Trims offset voltage of HPL** 0000: 0V 0001: -0.5mV 0010: -1.5mV 0011: -2.5mV 0100: -3.5mV 0101: -4.5mV 0110: -5.5mV 0111: -6.5mV 1001: 0.5mV 1010: 1.5mV 1011: 2.5mV 1100: 3.5mV 1101: 4.5mV 1110: 5.5mV 1111: 6.5mV
2	RG_HSOUT_SHORTVCM_VAUDP15	**Shorts HS output to VCM (DCC: 0V; ACC: 1.4V)** 0: Does not short to VCM 1: Short to VCM
1:0	RG_HPOUTSTB_RSEL_VAUDP15	**Selects OUTSTB resistance** 00: 250 01: 470 10: 1.5k

0CE2 **AUDDEC_ANA_CON3** **AUDDEC Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUDHPSPKDET_OUTPUTMUXSEL_VAUDP15		RG_AUDHPSPKDET_INPUTMUXSEL_VAUDP15		RG_AUDHPSPKDET_EN_VAUDP15	RG_AUDTRIMBUF_GAINSEL_VAUDP15		RG_AUDTRIMBUF_INPUTMUXSEL_VAUDP15				RG_AUDTRIMBUF_EN_VAUDP15
Type					RW		RW		RW	RW		RW				RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
11:10	RG_AUDHPSPKDET_OUTPUTMUXSEL_VAUDP15	**Selects audio headphone speaker detection output mux** 00: Open 01: HPL 10: HPR 11: Unused
9:8	RG_AUDHPSPKDET_INPUTMUXSEL_VAUDP15	**Enables audio headphone speaker detection input mux** 00: Open 01: DACLP 10: DACLN 11: DACRP
7	RG_AUDHPSPKDET_EN_VAUDP15	**Enables audio headphone speaker detection**
6:5	RG_AUDTRIMBUF_GAINSEL_VAUDP15	**Selects audio offset trimming buffer gain** 00: 0dB 01: 6dB 10: 12dB 11: 18dB
4:1	RG_AUDTRIMBUF_INPUTMUXSEL_VAUDP15	**Selects audio offset trimming buffer mux** 0000: Open 0001: HPL 0010: HPR 0011: HSP 0100: HSN 0101: IV_P 0110: IV_N 0111: AVSS32 1000: AVSS32 1001: AVSS32 1010~1111: Unused
0	RG_AUDTRIMBUF_EN_VAUDP15	**Enables audio offset trimming buffer**

0CE4 AUDDEC_ANA_CON4 AUDDEC Control Register 4 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ABIDEC_RESERVED_VAUDP15								RG_ABIDEC_RESERVED_VA28							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	RG_ABIDEC_RESERVED_VAUDP15	Reserved one byte in VAUDP15 domain
7:0	RG_ABIDEC_RESERVED_VA28	Reserved one byte in VA28 domain

0CE6 AUDDEC_ANA_CON5 AUDDEC Control Register 5 5520

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDBIASADJ_1_VAUDP15						RG_AUDBIASADJ_0_VAUDP15									
Type	RW						RW									

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Reset	0	1	0	1	0	1	0	1	0	0	1	0				

Bit(s)	Name	Description
15:10	RG_AUDBIASADJ_1_VAUDP15	**Audio bias adjustment 1** [5:4] ZCD bias current setting 00: 3uA 01: 4uA 10: 5uA 11: 6uA [3:2] HS ibias setting 00: 4uA 01: 5uA 10: 6uA 11: 7uA [1:0]: HPL/R ibias setting 00: 4uA 01: 5uA 10: 6uA 11: 7uA
9:4	RG_AUDBIASADJ_0_VAUDP15	**Audio bias adjustment 0** [2:0] Headphone left/right DR bias current setting [5:3] Handset DR bias current setting. DR bias settings: 000: 4uA 001: 5uA 010: 6uA 011: 7uA 100: 8uA 101: 9A 110: 10uA 111: 11uA,

0CE8 AUDDEC_ANA_CON6 AUDDEC Control Register 6 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_HCLDO_VOSEL_VA18**	**RG_LCLDO_VOSEL_VA18**	**RG_LCLDO_REMOTE_SENSE_VA18**	**RG_LCLDO_PDDIS_EN_VA18**	**RG_HCLDO_REMOTE_SENSE_VA18**	**RG_HCLDO_PDDIS_EN_VA18**	**RG_VA33REFGEN_EN_VA18**	**RG_LCLDO_ENC_EN_VA28**	**RG_LCLDO_EN_VA18**	**RG_HCLDO_EN_VA18**	**RG_SEL_DELAY_VCORE**	**RG_SEL_ENCODER_96K_VA28**	**RG_SEL_DECODER_96K_VA28**	**RG_RSTB_ENCODER_VA28**	**RG_RSTB_DECODER_VA28**	**RG_AUDIBIASPWRDN_VAUDP15**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15	RG_HCLDO_VOSEL_VA18	
14	RG_LCLDO_VOSEL_VA18	
13	RG_LCLDO_REMOTE_SENSE_VA18	**Selects LCLDO remote sense function**
12	RG_LCLDO_PDDIS	**Enables LCLDO power-down discharge**

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Bit(s)	Name	Description
	_EN_VA18	
11	RG_HCLDO_REMOTE_SENSE_VA18	**Selects HCLDO remote sense function** 0: Local sense 1: Remote sense
10	RG_HCLDO_PDDIS_EN_VA18	**Enables HCLDO power-down discharge**
9	RG_VA33REFGEN_EN_VA18	
8	RG_LCLDO_ENC_EN_VA28	**Enables LCLDO_ENC**
7	RG_LCLDO_EN_VA18	**Enables LCLDO**
6	RG_HCLDO_EN_VA18	**Enables HCLDO**
5	RG_SEL_DELAY_VCORE	**Selects AFIFO read clock delay** 0: 5ns 1: 10ns
4	RG_SEL_ENCODER_96K_VA28	**Selects audio ADC clock** 0: 6.5MHz 1: 13MHz
3	RG_SEL_DECODER_96K_VA28	**Selects audio DAC clock** 0: 6.5MHz 1: 13MHz
2	RG_RSTB_ENCODER_VA28	**Resets audio encoder** 0: Reset 1: Normal
1	RG_RSTB_DECODER_VA28	**Resets audio decoder** 0: Reset 1: Normal
0	RG_AUDIBIASPWRDN_VAUDP15	**Controls power-down for IbiasDistrib circuit.** 0: Enable 1: Disable

0CEA **AUDDEC_ANA_CON7** **AUDDEC Control Register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_NVREG_EN_VAUDP15	RG_AUDPMU_RESERVED_VAUDP15				RG_AUDPMU_RESERVED_VA18				RG_AUDPMU_RESERVED_VA28				RG_VA28REFGEN_EN_VA28	RG_LCLDO_ENC_REMOTE_SENSE_VA28	RG_LCLDO_ENC_PDDIS_EN_VA28
Type	RW	RW				RW				RW				RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RG_NVREG_EN_V	Enables NVREG

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Bit(s)	Name	Description
	AUDP15	
14:11	RG_AUDPMU_RESERVED_VAUDP15	Reserved half byte for VAUDP15 domain
10:7	RG_AUDPMU_RESERVED_VA18	Reserved half byte for VA18 domain
6:3	RG_AUDPMU_RESERVED_VA28	Reserved half byte for VA28 domain
2	RG_VA28REFGEN_EN_VA28	Enables VA28 Ref. gen.
1	RG_LCLDO_ENC_REMOTE_SENSE_VA28	Selects LCLDO_ENC remote sense function
0	RG_LCLDO_ENC_PDDIS_EN_VA28	Enables LCLDO_ENC power-down discharge

0CEC **AUDDEC_ANA_CON8** **AUDDEC Control Register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_AUDGLB_PWRDN_VA28	RG_NVREG_PULL0V_VAUDP15
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_AUDGLB_PWRDN_VA28	**Controls power-down for audio global bias circuit** 0: Enable 1: Disable; default on
0	RG_NVREG_PULL0V_VAUDP15	0: DCC mode. Switch is opened; NV output is -0.95V 1: ACC mode. Switch is closed; NV reg output is pulled to GND.

0CEE **AUDENC_ANA_CON0** **AUDENC Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_AUDADCLINPUTSEL		RG_AUDADCLPWRUP	RG_AUDPREAMPLINPUTSEL		RG_AUDPREAMPLVSCALE		RG_AUDPREAMPLPGATEST	RG_AUDPREAMPLDCRPECHARGE	RG_AUDPREAMPLDCEN	RG_AUDPREAMPLON
Type						RW		RW	RW		RW		RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
10:9	RG_AUDADCLINPUTSEL	**Selects audio L ADC input** 00: Idle 01: AIN0 10: Left preamplifier 11: Idle
8	RG_AUDADCLPWRUP	**Powers up audio L ADC** 0: Power down 1: Power on
7:6	RG_AUDPREAMPLINPUTSEL	**Selects audio L preamplifier input** 00: None 01: AIN0 10: AIN1 11: AIN2
5:4	RG_AUDPREAMPLVSCALE	**Audio L preamplifier PGA DC output voltage scale**
3	RG_AUDPREAMPLPGATEST	**Enables audio L preamplifier PGA test** 0: Disable 1: Enable
2	RG_AUDPREAMPLDCRPECHARGE	**Audio L preamplifier PGA DC couple input precharge** 0: Disable 1: Enable
1	RG_AUDPREAMPLDCCEN	**Audio L DC couple input** 0: AC couple input 1: DC couple input
0	RG_AUDPREAMPLON	**Enables audio L preamplifier** 0: Disable 1: Enable

0CF0 **AUDENC_ANA_CON1** **AUDENC Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_AUDADCRINPUTSEL		RG_AUDADCRPWRUP	RG_AUDPREAMPRINPUTSEL		RG_AUDPREAMPRVSCALE		RG_AUDPREAMPRPGATEST	RG_AUDPREAMPRDCRPECHARGE	RG_AUDPREAMPRDCCEN	RG_AUDPREAMPRON
Type						RW		RW	RW		RW		RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10:9	RG_AUDADCRINPUTSEL	**Selects audio R ADC input** 00: Idle 01: AIN0 10: Right preamplifier 11: Idle
8	RG_AUDADCRPWRUP	**Powers up audio R ADC** 0: Power down 1: Power on

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Bit(s)	Name	Description
7:6	RG_AUDPREAMPR INPUTSEL	**Selects audio R preamplifier input** 00: None 01: AIN0 10: AIN1 11: AIN2
5:4	RG_AUDPREAMPR VSCALE	**Audio R preamplifier PGA DC output voltage scale**
3	RG_AUDPREAMPR PGATEST	**Enables audio R preamplifier PGA test** 0: Disable 1: Enable
2	RG_AUDPREAMPR DCRPECHARGE	**Audio R preamplifier PGA DC couple input precharge** 0: Disable 1: Enable
1	RG_AUDPREAMPR DCCEN	**Audio R DC couple input** 0: AC couple input 1: DC couple input
0	RG_AUDPREAMPR ON	**Enables audio R preamplifier** 0: Disable 1: Enable

0CF2 **AUDENC_ANA_CON2** **AUDENC Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDADCFLASHIDDTEST		RG_AUDADCREFBUFIDDTEST		RG_AUDADC2NDSTAGEIDDTEST		RG_AUDADC1STSTAGEIDDTEST		RG_AUDPREAMPIDDTEST		RG_AUDADCFLASHLPEN	RG_AUDADC2NDSTAGELPEN	RG_AUDADC1STSTAGELPEN	RG_AUDPREAMPLPEN	RG_AUDGLBMADLPWEN	RG_AUDULHALFBIAS
Type	RW		RW		RW		RW		RW		RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:14	RG_AUDADCFLASHIDDTEST	**Selects audio ADC flash Idd current test** 00: 100% 01: 80% 10: 120% 11: 140%
13:12	RG_AUDADCREFBUFIDDTEST	**Selects audio ADC reference buffer Idd current test** 00: 100% 01: 80% 10: 120% 11: 140%
11:10	RG_AUDADC2NDSTAGEIDDTEST	**Adjusts audio ADC 2nd & 3rd stage Idd** 00: 100% 01: 80% 10: 120% 11: 140%
9:8	RG_AUDADC1STSTAGEIDDTEST	**Adjusts audio ADC 1st stage Idd** 00: 100% 01: 80%

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Bit(s)	Name	Description
		10: 120% 11: 140%
7:6	RG_AUDPREAMPIDDTEST	**Adjusts audio preamplifier Idd** 00: 100% 01: 75% 10: 125% 11: 150%
5	RG_AUDADCFLASHLPEN	**Enables audio ADC flash low power** 0: Normal 1: Enable
4	RG_AUDADC2NDSTAGELPEN	**Enables audio ADC 2nd & 3rd low power** 0: Normal 1: Enable
3	RG_AUDADC1STSTAGELPEN	**Enables audio ADC 1st stage low power** 0: Normal 1: Enable
2	RG_AUDPREAMPLPEN	**Audio preamplifier PGA low power mode** 0: Disable 1: Enable
1	RG_AUDGLBMADLPWEN	**Audio preamplifier PGA low power mode** 0: Disable 1: Enable
0	RG_AUDULHALFBIAS	**Enables audio uplink halfbias** 0: Normal 1: Enable

0CF4 AUDENC_ANA_CON3 AUDENC Control Register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_AUDSPAREPGA	RG_DCCVCMBUFLPSWEN	RG_DCCVCMBUFLPMODSEL	RG_AUDPREAMPAAFEN			RG_AUDADCCLKGENMODE		RG_AUDADCCLKSOURCE		RG_AUDADCCLKSEL	RG_AUDADCDAC0P25FS
Type					RW	RW	RW	RW			RW		RW		RW	RW
Reset					0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
11	RG_AUDSPAREPGA	**Spare control bits for PGA**
10	RG_DCCVCMBUFLPSWEN	**Enables audio preamplifier PGA DCC VCM buffer SW**
9	RG_DCCVCMBUFLPMODSEL	**Audio preamplifier PGA DCC VCM buffer LP MODSEL**
8	RG_AUDPREAMPAAFEN	**Audio preamplifier PGA with AAF input in DC couple mode** 0: Disable 1: Enable
5:4	RG_AUDADCCLKGENMODE	**Audio ADC clock gen. mode** 00: Divided by 2 (normal)

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Bit(s)	Name	Description
		01: Divided by 4 10: Divided by 8 11: Not divided
3:2	RG_AUDADCCLKSOURCE	**Audio ADC clock source** 00: 26MHz from CLKSQ 01: 12.58MHz from 32kHz PLL 10: 12MHz Ring oscillator 11: None
1	RG_AUDADCCLKSEL	**Selects audio ADC clock** 0: 13MHz clock in; 6.5MHz data out 1: 26MHz clock in; 13MHz data out
0	RG_AUDADCDAC0P25FS	**Enables audio ADC FBDAC 0.25FS** 0: 13MHz clock in; 6.5MHz data out 1: 3.25MHz clock in; 1.625MHz data out

0CF6 **AUDENC_ANA_CON4** **AUDENC Control Register 4** **0800**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_AUDADCDACTEST	RG_AUDADCNODEM	RG_AUDADCDACNRZ	RG_AUDADCDACIDDTEST		RG_AUDADCDACFBCURRENT	RG_AUDADCFFBYPASS	RG_AUDADCBYPASS	RG_AUDADCNOPATEST	RG_AUDADCWIDECM	RG_AUDADCFSRESET	RG_AUDADC3RDSTAGERESET	RG_AUDADC2NDSTAGERESET	RG_AUDADC1STSTAGESDENB
Type			RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset			0	0	1	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13	RG_AUDADCDACTEST	**Audio ADC DAC test** 0: Disable 1: Enable data in RG_AUDADCTESTDATA[15:0] to be passed to DAC
12	RG_AUDADCNODEM	**Audio ADC DEM test**
11	RG_AUDADCDACNRZ	**Audio ADC DAC in non return to zero mode** 0: RZ mode (2I) 1: NRZ mod (I)
10:9	RG_AUDADCDACIDDTEST	**Selects audio ADC-DAC Idd current test** 00: Normal 11: -20% DAC f/b current
8	RG_AUDADCDACFBCURRENT	**Audio ADC feedback coefficient**
7	RG_AUDADCFFBYPASS	**Bypasses audio ADC feed forward** 0: No bypass. Allow feedforward coefficient to pass signal to ADC flash. 1: Bypass. Does not allow ADC i/p signal to feedforward flash.
6	RG_AUDADCBYPASS	**Enables audio ADC input resistor bypass** 0: Disable 1: Enable
5	RG_AUDADCNOPATEST	**Audio ADC no preamp test** 0: Normal ADC gain

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Bit(s)	Name	Description
		1: 6dB ADC gain
4	RG_AUDADCWIDECM	**Enables audio ADC wide common mode** 0: Normal 1: Enable
3	RG_AUDADCFSRESET	**Selects audio encoder FS reset block model**
2	RG_AUDADC3RDSTAGERESET	**Resets audio ADC 3rd stage** 0: Normal 1: Reset
1	RG_AUDADC2NDSTAGERESET	**Resets audio ADC 2nd stage** 0: Normal 1: Reset
0	RG_AUDADC1STSTAGESDENB	**Audio ADC 1st stage source degenerate enableb** 0: Enable 1: Disable

0CF8 **AUDENC_ANA_CON5** **AUDENC Control Register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDADCTESTDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RG_AUDADCTESTDATA	**Audio ADC test data bits for both phases of DRTZ DAC** Can enable any current source you choose.

0CFA **AUDENC_ANA_CON6** **AUDENC Control Register 6** **0555**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_AUDRCTUNERSEL			RG_AUDRCTUNER					RG_AUDRCTUNELSEL	RG_AUDRCTUNEL				
Type			RW			RW					RW	RW				
Reset			0			1	0	1	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
13	RG_AUDRCTUNERSEL	**Selects audio R ADC RC tuning** 0: Use auto cal tune bits 1: Use RG_AUDRCTUNEL[4:0]
10:6	RG_AUDRCTUNER	**Audio R ADC RC tuned value** See RG_AUDRCTUNELSE.
5	RG_AUDRCTUNELSEL	**Selects audio L ADC RC tuning** 0: Use auto cal tune bits 1: Use RG_AUDRCTUNEL[4:0]

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Bit(s)	Name	Description
4:0	RG_AUDRCTUNEL	**Audio L ADC RC tuned value** See RG_AUDRCTUNELSE.

0CFC AUDENC_ANA_CON7 AUDENC Control Register 7 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDENCSPAREVA18				RG_AUDENCSPAREVA28				RG_AUDSPAREVA18				RG_AUDSPAREVA28			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:12	RG_AUDENCSPAREVA18	Spare control bits for AVDD12 voltage domain
11:8	RG_AUDENCSPAREVA28	Spare control bits for AVDD25 voltage domain
7:4	RG_AUDSPAREVA18	Spare control bits for AVDD12 voltage domain
3:0	RG_AUDSPAREVA28	Spare control bits for AVDD25 voltage domain

0CFE AUDENC_ANA_CON8 AUDENC Control Register 8 0004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDSPAREVMIC				RG_DMICMONSEL			RG_DMICMONEN	RG_AUDDIGMICNDUTY		RG_AUDDIGMICPDUTY		RG_DMICHPCLKEN	RG_AUDDIGMICBIAS		RG_AUDDIGMICEN
Type	RW				RW			RW	RW		RW		RW	RW		RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
15:12	RG_AUDSPAREVMIC	**Spare control bits for AVDD25MIC voltage domain**
11:9	RG_DMICMONSEL	**Enables digital microphone monitor path** 0: Disable 1: Enable
8	RG_DMICMONEN	**Enables digital microphone monitor path** 0: Disable 1: Enable (26MHz)
7:6	RG_AUDDIGMICNDUTY	**Controls digital microphone negative duty**
5:4	RG_AUDDIGMICPDUTY	**Controls digital microphone positive duty**
3	RG_DMICHPCLKEN	**Enables digital microphone monitor path selection** 0: DCC CLK 1: CLKSQ

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Bit(s)	Name	Description
2:1	RG_AUDDIGMICBIAS	**Controls digital microphone slew rate** 11>10>01>00
0	RG_AUDDIGMICEN	**Enables digital microphone** 0: Disable 1: Enable

0D00 **AUDENC_ANA_CON9** **AUDENC Control Register 9** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**RG_BANDGAPGEN**	**RG_AUDMICBIASLOWPEN**	**RG_AUDMICBIASVREF**			**RG_AUDMICBIAS1BYPASSEN**	**RG_AUDMICBIAS1DCSWNEN**	**RG_AUDMICBIAS1DCSWPEN**	**RG_AUDPWDBMICBIAS1**	**RG_AUDMICBIAS0BYPASSEN**	**RG_AUDMICBIAS0DCSWNEN**	**RG_AUDMICBIAS0DCSWPEN**	**RG_AUDPWDBMICBIAS0**
Type				RW	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12	RG_BANDGAPGEN	**Remote sense to bandgap ground** 0: Disable 1: Enable
11	RG_AUDMICBIASLOWPEN	**Enables MIC Bias 0 low power** 0: High power mode 1: Low power mode
10:8	RG_AUDMICBIASVREF	**Selects MIC Bias 0 output voltage selection** 000: 1.7V 001: 1.8V 010: 1.9V 011: 2.0V 100: 2.1V 101: 2.3V 110: 2.4V 111: 2.5V
7	RG_AUDMICBIAS1BYPASSEN	**Enables MIC Bias 1 bypass 2P8V** 0: Disable 1: Enable
6	RG_AUDMICBIAS1DCSWNEN	**MIC Bias 1 DC couple switch N** 0: External 1: Internal
5	RG_AUDMICBIAS1DCSWPEN	**MIC Bias 1 DC couple switch P** 0: External 1: Internal
4	RG_AUDPWDBMICBIAS1	**Powers down MIC Bias 1** 0: Power down 1: Power on
3	RG_AUDMICBIAS0BYPASSEN	**Enables MIC Bias 0 bypass 2P8V** 0: Disable 1: Enable
2	RG_AUDMICBIAS0	**MIC Bias 0 DC couple switch N**

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Bit(s)	Name	Description
	DCSWNEN	0: External 1: Internal
1	RG_AUDMICBIAS0DCSWPEN	**MIC Bias 0 DC couple switch P** 0: External 1: Internal
0	RG_AUDPWDBMICBIAS0	**Powers down MIC Bias 0** 0: Power down 1: Power on

0D02 AUDENC_ANA_CON10 AUDENC Control Register 10 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_AUDPREAMPRGAIN				RG_AUDPREAMPLGAIN		
Type										RW				RW		
Reset										0	0	0		0	0	0

Bit(s)	Name	Description
6:4	RG_AUDPREAMPRGAIN	**Adjusts audio R preamplifier gain** 000: 0dB 001: 6dB 010: 12dB 011: 18dB 100: 24dB
2:0	RG_AUDPREAMPLGAIN	**Adjusts audio L preamplifier gain** 000: 0dB 001: 6dB 010: 12dB 011: 18dB 100: 24dB

0D04 AUDNCP_CLKDIV_CON0 AUDNCP_CLKDIV Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_DIVCKS_CHG
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_DIVCKS_CHG	

0D06 AUDNCP_CLKDIV_CON1 AUDNCP_CLKDIV Control Register 1 0000

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_DIVCKS_ON
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_DIVCKS_ON	

0D08 **AUDNCP_CLKDIV_CON2** **AUDNCP_CLKDIV Control Register 2** **0020**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_DIVCKS_PRG								
Type								RW								
Reset								0	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
8:0	RG_DIVCKS_PRG	

0D0A **AUDNCP_CLKDIV_CON3** **AUDNCP_CLKDIV Control Register 3** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_DIVCKS_PWD_NCP
Type																RW
Reset																1

Bit(s)	Name	Description
0	RG_DIVCKS_PWD_NCP	

0D0C **AUDNCP_CLKDIV_CON4** **AUDNCP_CLKDIV Control Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_DIVCKS_PWD_NCP_ST_SEL	
Type															RW	
Reset															0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
1:0	RG_DIVCKS_PWD_NCP_ST_SEL	

0E00	AUXADC_ADC0	AUXADC ADC Register 0	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH0	AUXADC_ADC_OUT_CH0														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0	**AUXADC channel 0 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0	**AUXADC channel 0 output data**

0E02	AUXADC_ADC1	AUXADC ADC Register 1	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH1	AUXADC_ADC_OUT_CH1														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1	**AUXADC channel 1 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1	**AUXADC channel 1 output data**

0E04	AUXADC_ADC2	AUXADC ADC Register 2	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_R				AUXADC_ADC_OUT_CH2											

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	DY_CH2															
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH2	**AUXADC channel 2 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH2	**AUXADC channel 2 output data**

0E06 AUXADC_ADC3 AUXADC ADC Register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH3				AUXADC_ADC_OUT_CH3											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH3	**AUXADC channel 3 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH3	**AUXADC channel 3 output data**

0E08 AUXADC_ADC4 AUXADC ADC Register 4 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH4				AUXADC_ADC_OUT_CH4											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH4	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH4	**AUXADC channel 4 output data**

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0E0A **AUXADC_ADC5** **AUXADC ADC Register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH5				AUXADC_ADC_OUT_CH5											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH5	**AUXADC channel 5 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH5	**AUXADC channel 5 output data**

0E0C **AUXADC_ADC6** **AUXADC ADC Register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH6				AUXADC_ADC_OUT_CH6											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH6	**AUXADC channel 6 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH6	**AUXADC channel 6 output data**

0E0E **AUXADC_ADC7** **AUXADC ADC Register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7	AUXADC_ADC_OUT_CH7														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7	**AUXADC channel 7 output data**

0E10 **AUXADC_ADC8** **AUXADC ADC Register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH8				AUXADC_ADC_OUT_CH8											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH8	**AUXADC channel 8 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH8	**AUXADC channel 8 output data**

0E12 **AUXADC_ADC9** **AUXADC ADC Register 9** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH9				AUXADC_ADC_OUT_CH9											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH9	**AUXADC channel 9 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH9	**AUXADC channel 9 output data**

0E14 **AUXADC_ADC10** **AUXADC ADC Register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	AUXADC_ADC_RDY_CH10				AUXADC_ADC_OUT_CH10											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH10	**AUXADC channel 10 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH10	**AUXADC channel 10 output data**

0E16 **AUXADC_ADC11** **AUXADC ADC Register 11** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH11				AUXADC_ADC_OUT_CH11											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH11	**AUXADC channel 11 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH11	**AUXADC channel 11 output data**

0E18 **AUXADC_ADC12** **AUXADC ADC Register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH12_15				AUXADC_ADC_OUT_CH12_15											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH12_15	**AUXADC channel 12_15 output data ready** 0: AUXADC data proceeding

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Bit(s)	Name	Description
		1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH12_15	**AUXADC channel 12_15 output data**

0E1A **AUXADC_ADC13** **AUXADC ADC Register 13** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_RDY_THR_HW**				**AUXADC_ADC_OUT_THR_HW**											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_THR_HW	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_THR_HW	**AUXADC channel 4 output data**

0E1C **AUXADC_ADC14** **AUXADC ADC Register 14** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_RDY_LBAT**				**AUXADC_ADC_OUT_LBAT**											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_LBAT	**AUXADC low battery output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_LBAT	**AUXADC low battery output data**

0E1E **AUXADC_ADC15** **AUXADC ADC Register 15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	**AUXADC_ADC_RDY_LBAT2**				**AUXADC_ADC_OUT_LBAT2**											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_LBAT2	**AUXADC low battery output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_LBAT2	**AUXADC low battery output data**

0E20 **AUXADC_ADC16** **AUXADC ADC Register 16** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_RDY_CH7_BY_GPS**	**AUXADC_ADC_OUT_CH7_BY_GPS**														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7_BY_GPS	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7_BY_GPS	**AUXADC channel 7 output data**

0E22 **AUXADC_ADC17** **AUXADC ADC Register 17** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_ADC_RDY_CH7_BY_MD**	**AUXADC_ADC_OUT_CH7_BY_MD**														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7_BY_MD	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7_BY_MD	**AUXADC channel 7 output data**

0E24 **AUXADC_ADC18** **AUXADC ADC Register 18** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7_BY_AP	AUXADC_ADC_OUT_CH7_BY_AP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7_BY_AP	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7_BY_AP	**AUXADC channel 7 output data**

0E26 **AUXADC_ADC19** **AUXADC ADC Register 19** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH4_BY_MD				AUXADC_ADC_OUT_CH4_BY_MD											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH4_BY_MD	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH4_BY_MD	**AUXADC channel 4 output data**

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0E28 **AUXADC_ADC20** **AUXADC ADC Register 20** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_WAKEUP_PCHR	AUXADC_ADC_OUT_WAKEUP_PCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_WAKEUP_PCHR	**AUXADC wakeup output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_WAKEUP_PCHR	**AUXADC wakeup output data**

0E2A **AUXADC_ADC21** **AUXADC ADC Register 21** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_WAKEUP_SWCHR	AUXADC_ADC_OUT_WAKEUP_SWCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_WAKEUP_SWCHR	**AUXADC wakeup output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_WAKEUP_SWCHR	**AUXADC wakeup output data**

0E2C **AUXADC_ADC22** **AUXADC ADC Register 22** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_R	AUXADC_ADC_OUT_CH0_BY_MD														

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	DY_ CH0 _BY _MD	
Type	RO	RO
Reset	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0_BY_MD	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0_BY_MD	**AUXADC channel output data**

0E2E **AUXADC_ADC23** **AUXADC ADC Register 23** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH0_BY_AP	AUXADC_ADC_OUT_CH0_BY_AP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0_BY_AP	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0_BY_AP	**AUXADC channel output data**

0E30 **AUXADC_ADC24** **AUXADC ADC Register 24** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH1_BY_MD	AUXADC_ADC_OUT_CH1_BY_MD														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1_BY_MD	**AUXADC channel output data ready** 0: AUXADC data proceeding

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Bit(s)	Name	Description
		1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1_BY_MD	**AUXADC channel output data**

0E32 **AUXADC_ADC25** **AUXADC ADC Register 25** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH1_BY_AP	AUXADC_ADC_OUT_CH1_BY_AP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1_BY_AP	**AUXADC channel output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1_BY_AP	**AUXADC channel output data**

0E34 **AUXADC_ADC26** **AUXADC ADC Register 26** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_VISMPS0				AUXADC_ADC_OUT_VISMPS0											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_VISMPS0	**AUXADC vismps output data ready** 0: AUXADC vismps data proceeding 1: AUXADC vismps data ready
11:0	AUXADC_ADC_OUT_VISMPS0	**AUXADC vismps output data**

0E36 **AUXADC_ADC27** **AUXADC ADC Register 27** **0000**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_FGADC1	AUXADC_ADC_OUT_FGADC1														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_FGADC1	**AUXADC output data ready (BATSNS)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_FGADC1	**AUXADC output data**

0E38 AUXADC_ADC28 AUXADC ADC Register 28 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_FGADC2	AUXADC_ADC_OUT_FGADC2														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_FGADC2	**AUXADC output data ready (ISENSE)** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_FGADC2	**AUXADC output data**

0E3A AUXADC_ADC29 AUXADC ADC Register 29 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_IMP	AUXADC_ADC_OUT_IMP														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RD	**AUXADC output data ready**

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Bit(s)	Name	Description
	Y_IMP	0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_IMP	**AUXADC output data**

0E3C **AUXADC_ADC30** **AUXADC ADC Register 30** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_IMP_AVG	AUXADC_ADC_OUT_IMP_AVG														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_IMP_AVG	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_IMP_AVG	**AUXADC output data**

0E3E **AUXADC_ADC31** **AUXADC ADC Register 31** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		AUXADC_ADC_OUT_RAW														
Type		RO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:0	AUXADC_ADC_OUT_RAW	AUXADC channel output raw data

0E40 **AUXADC_ADC32** **AUXADC ADC Register 32** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_MDRT	AUXADC_ADC_OUT_MDRT														
Type	RO	RO														

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_MDRT	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_MDRT	**AUXADC output data**

0E42 **AUXADC_ADC33** **AUXADC ADC Register 33** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_MDBG	AUXADC_ADC_OUT_MDBG														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_MDBG	**AUXADC output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_MDBG	**AUXADC output data**

0E44 **AUXADC_BUF0** **AUXADC_BUF0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_00	AUXADC_BUF_OUT_00														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_00	**AUXADC_BUF_00** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_00	

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0E46	AUXADC_BUF1	AUXADC_BUF1	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_01	AUXADC_BUF_OUT_01														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_01	**AUXADC_BUF_01** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_01	

0E48	AUXADC_BUF2	AUXADC_BUF2	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_02	AUXADC_BUF_OUT_02														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_02	**AUXADC_BUF_02** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_02	

0E4A	AUXADC_BUF3	AUXADC_BUF3	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_03	AUXADC_BUF_OUT_03														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15	AUXADC_BUF_RDY_03	**AUXADC_BUF_03** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_03	

0E4C **AUXADC_BUF4** **AUXADC_BUF4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_04	AUXADC_BUF_OUT_04														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_04	**AUXADC_BUF_04** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_04	

0E4E **AUXADC_BUF5** **AUXADC_BUF5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_05	AUXADC_BUF_OUT_05														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_05	**AUXADC_BUF_05** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_05	

0E50 **AUXADC_BUF6** **AUXADC_BUF6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	AUXADC_BUF_RDY_06	AUXADC_BUF_OUT_06														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_06	**AUXADC_BUF_06** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_06	

0E52 **AUXADC_BUF7** **AUXADC_BUF7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_07	AUXADC_BUF_OUT_07														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_07	**AUXADC_BUF_07** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_07	

0E54 **AUXADC_BUF8** **AUXADC_BUF8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_08	AUXADC_BUF_OUT_08														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_08	**AUXADC_BUF_08** 0: AUXADC data proceeding 1: AUXADC data ready

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Bit(s)	Name	Description
14:0	AUXADC_BUF_OUT_08	

0E56 **AUXADC_BUF9** **AUXADC_BUF9** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_09	AUXADC_BUF_OUT_09														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_09	**AUXADC_BUF_09** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_09	

0E58 **AUXADC_BUF10** **AUXADC_BUF10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_10	AUXADC_BUF_OUT_10														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_10	**AUXADC_BUF_10** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_10	

0E5A **AUXADC_BUF11** **AUXADC_BUF11** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_R	AUXADC_BUF_OUT_11														

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	DY_11															
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_11	**AUXADC_BUF_11** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_11	

0E5C AUXADC_BUF12 AUXADC_BUF12 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_12	AUXADC_BUF_OUT_12														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_12	**AUXADC_BUF_12** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_12	

0E5E AUXADC_BUF13 AUXADC_BUF13 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_13	AUXADC_BUF_OUT_13														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_13	**AUXADC_BUF_13** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_13	

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0E60	AUXADC_BUF14	AUXADC_BUF14	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_14	AUXADC_BUF_OUT_14														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_14	**AUXADC_BUF_14** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_14	

0E62	AUXADC_BUF15	AUXADC_BUF15	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_15	AUXADC_BUF_OUT_15														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_15	**AUXADC_BUF_15** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_15	

0E64	AUXADC_BUF16	AUXADC_BUF16	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_16	AUXADC_BUF_OUT_16														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	AUXADC_BUF_RDY_16	**AUXADC_BUF_16** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_16	

0E66	AUXADC_BUF17	AUXADC_BUF17	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_17	AUXADC_BUF_OUT_17														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_17	**AUXADC_BUF_17** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_17	

0E68	AUXADC_BUF18	AUXADC_BUF18	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_18	AUXADC_BUF_OUT_18														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_18	**AUXADC_BUF_18** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_18	

0E6A	AUXADC_BUF19	AUXADC_BUF19	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	AUXADC_BUF_RDY_19	AUXADC_BUF_OUT_19														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_19	**AUXADC_BUF_19** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_19	

0E6C **AUXADC_BUF20** **AUXADC_BUF20** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_20	AUXADC_BUF_OUT_20														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_20	**AUXADC_BUF_20** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_20	

0E6E **AUXADC_BUF21** **AUXADC_BUF21** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_21	AUXADC_BUF_OUT_21														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_21	**AUXADC_BUF_21** 0: AUXADC data proceeding 1: AUXADC data ready

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Bit(s)	Name	Description
14:0	AUXADC_BUF_OUT_21	

0E70 **AUXADC_BUF22** **AUXADC_BUF22** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_22	AUXADC_BUF_OUT_22														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_22	**AUXADC_BUF_22** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_22	

0E72 **AUXADC_BUF23** **AUXADC_BUF23** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_23	AUXADC_BUF_OUT_23														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_23	**AUXADC_BUF_23** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_23	

0E74 **AUXADC_BUF24** **AUXADC_BUF24** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_R	AUXADC_BUF_OUT_24														

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	DY_ 24															
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_24	**AUXADC_BUF_24** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_24	

0E76 AUXADC_BUF25 AUXADC_BUF25 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_BUF_RDY_25**	**AUXADC_BUF_OUT_25**														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_25	**AUXADC_BUF_25** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_25	

0E78 AUXADC_BUF26 AUXADC_BUF26 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**AUXADC_BUF_RDY_26**	**AUXADC_BUF_OUT_26**														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_26	**AUXADC_BUF_26** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_26	

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0E7A **AUXADC_BUF27** **AUXADC_BUF27** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_27	AUXADC_BUF_OUT_27														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_27	**AUXADC_BUF_27** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_27	

0E7C **AUXADC_BUF28** **AUXADC_BUF28** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_28	AUXADC_BUF_OUT_28														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_28	**AUXADC_BUF_28** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_28	

0E7E **AUXADC_BUF29** **AUXADC_BUF29** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_29	AUXADC_BUF_OUT_29														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15	AUXADC_BUF_RDY_29	**AUXADC_BUF_29** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_29	

0E80 **AUXADC_BUF30** **AUXADC_BUF30** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_30	AUXADC_BUF_OUT_30														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_30	**AUXADC_BUF_30** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_30	

0E82 **AUXADC_BUF31** **AUXADC_BUF31** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_BUF_RDY_31	AUXADC_BUF_OUT_31														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_BUF_RDY_31	**AUXADC_BUF_31** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_BUF_OUT_31	

0E84 **AUXADC_STA0** **AUXADC_STA0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	AUXADC_ADC_BUSY_IN_WAKEUP	AUXADC_ADC_BUSY_IN_VISMPS0	AUXADC_ADC_BUSY_IN_LBAT2	AUXADC_ADC_BUSY_IN_LBAT	AUXADC_ADC_BUSY_IN											
Type	RO	RO	RO	RO	RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_BUSY_IN_WAKEUP	**ADC busy status** 0: Idle 1: Busy
14	AUXADC_ADC_BUSY_IN_VISMPS0	**ADC busy status** 0: Idle 1: Busy
13	AUXADC_ADC_BUSY_IN_LBAT2	**ADC busy status** 0: Idle 1: Busy
12	AUXADC_ADC_BUSY_IN_LBAT	**ADC busy status** 0: Idle 1: Busy
11:0	AUXADC_ADC_BUSY_IN	**AUXADC ADC busy status** bit[11] = CH11 ~ bit[0] = CH0 0: Idle 1: Busy

0E86 **AUXADC_STA1** **AUXADC_STA1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_BUSY_IN_THR_MD	AUXADC_ADC_BUSY_IN_THR_HW	AUXADC_ADC_BUSY_IN_GPS	AUXADC_ADC_BUSY_IN_GPS_MD	AUXADC_ADC_BUSY_IN_GPS_AP	AUXADC_ADC_BUSY_IN_FGADC2	AUXADC_ADC_BUSY_IN_FGADC1	AUXADC_ADC_BUSY_IN_IMP	AUXADC_ADC_BUSY_IN_SHARE	AUXADC_ADC_BUSY_IN_MDBG	AUXADC_ADC_BUSY_IN_MDRT					
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO					
Reset	0	0	0	0	0	0	0	0	0	0	0					

Bit(s)	Name	Description
15	AUXADC_ADC_BUSY_IN_THR_MD	**ADC busy status** 0: Idle 1: Busy
14	AUXADC_ADC_BUSY_IN_THR_HW	**ADC busy status** 0: Idle 1: Busy
13	AUXADC_ADC_BUSY_IN_GPS	**ADC busy status** 0: Idle

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Bit(s)	Name	Description
		1: Busy
12	AUXADC_ADC_BUSY_IN_GPS_MD	**ADC busy status** 0: Idle 1: Busy
11	AUXADC_ADC_BUSY_IN_GPS_AP	**ADC busy status** 0: Idle 1: Busy
10	AUXADC_ADC_BUSY_IN_FGADC2	**ADC busy status** 0: Idle 1: Busy
9	AUXADC_ADC_BUSY_IN_FGADC1	**ADC busy status** 0: Idle 1: Busy
8	AUXADC_ADC_BUSY_IN_IMP	**ADC busy status** 0: Idle 1: Busy
7	AUXADC_ADC_BUSY_IN_SHARE	**ADC busy status** 0: Idle 1: Busy
6	AUXADC_ADC_BUSY_IN_MDBG	**ADC busy status** 0: Idle 1: Busy
5	AUXADC_ADC_BUSY_IN_MDRT	**ADC busy status** 0: Idle 1: Busy

0EF4 **AUXADC_VISMPS0_5** **AUXADC_VISMPS0_5** **8000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AUXADC_VISMPS0_VOLT_MIN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	AUXADC_VISMPS0_VOLT_MIN	VISMPS0 detection voltage setting

0F02 **AUXADC_LBAT2_5** **AUXADC_LBAT2_5** **8000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AUXADC_LBAT2_VOLT_MIN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	AUXADC_LBAT2_VOLT_MIN	LBAT2 detection voltage setting

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0F14	ACCDET_CON0	ACCDET control register 0	0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_AUDACCDETMICBIAS0PULLLOW	AUDACCDETAUXADCSWCTRL_SEL		RG_AUDACCDETVIN1PULLLOW	RG_AUDACCDETTVDET	RG_AUDACCDETMICBIAS1PULLLOW	RG_AUDACCDETSWCTRL			RG_ACCDETSEL	RG_AUDACCDETANASWCTRLENB	RG_AUDACCDETVTHACAL	RG_AUDACCDETVTHBCAL
Type				RW	RW		RW	RW	RW	RW			RW	RW	RW	RW
Reset				0	0		0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
12	RG_AUDACCDETMICBIAS0PULLLOW	**Pulls low MIC Bias 0 pads when MICBIAS is off** 1'b0: Disable 1'b1: Enable
11	AUDACCDETAUXADCSWCTRL_SEL	1'b0: HW mode 1'b1: SW mode
9	RG_AUDACCDETVIN1PULLLOW	**Pulls low VIN1 pads when MICBIAS is off** 1'b0: Disable 1'b1: Enable
8	RG_AUDACCDETTVDET	**Places audio accessory detection into TV mode**
7	RG_AUDACCDETMICBIAS1PULLLOW	**Pulls low MIC Bias 1 pads when MICBIAS is off** 1'b0: Disable 1'b1: Enable
6:4	RG_AUDACCDETSWCTRL	**Controls ACCDET to AUXADC switch** 001: Normal mode 010: 200K 100: 100K Others: Not allowed
3	RG_ACCDETSEL	**Selects ACCDET input** 1'b0: ACCDET pin 1'b1: MICP pin
2	RG_AUDACCDETANASWCTRLENB	
1	RG_AUDACCDETVTHACAL	**Calibrates audio accessory detection voltage threshold A**
0	RG_AUDACCDETVTHBCAL	**Calibrates audio accessory detection voltage threshold B**

0F16	ACCDET_CON1	ACCDET Control Register 1	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										accdet_anasw	ACCDET_NE	ACCDET_NE	ACCDET_EIN	ACCDET_EI	ACCDET_SE	ACCDET_EN

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										ctrl_sel	GVDET_EN_CTRL	GVDET_EN	T_SEQ_INIT	NTDET_EN	Q_INIT	
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	accdet_anaswctrl_sel	**Selects who controls connection between AUXADC and ACCDET when in hook-key status** 1'b0: AUXADC 1'b1: ACCDET
5	ACCDET_NEGVDET_EN_CTRL	**Initializes status default value** 1'b0: HW mode 1'b1: SW mode
4	ACCDET_NEGVDET_EN	**Enables negative debounce** 1'b0: Disable 1'b1: Enable
3	ACCDET_EINT_SEQ_INIT	**Initializes EINT status default value** 1'b0: Disable 1'b1: Enable
2	ACCDET_EINTDET_EN	**Enables EINT detection** 1'b0: Disable 1'b1: Enable
1	ACCDET_SEQ_INIT	**Initializes ACCDET status default value** 1'b0: Normal mode 1'b1: Initialized mode
0	ACCDET_EN	**Enables ACCDET** Must be set to 0 before switched to TV mode. 1'b0: Disable 1'b1: Enable

0F18 **ACCDET_CON2** **ACCDET control register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													ACCDET_EINT_PWM_EN	ACCDET_MBIAS_PWM_EN	ACCDET_VTH_PWM_EN	ACCDET_CMP_PWM_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	ACCDET_EINT_PWM_EN	**Enables PWM of ACCDET EINT unit** Disabled in TV mode 1'b0: Disable 1'b1: Enable
2	ACCDET_MBIAS_PWM_EN	**Enables PWM of ACCDET MBIAS unit** Disabled in TV mode

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Bit(s)	Name	Description
		1'b0: Disable 1'b1: Enable
1	ACCDET_VTH_PWM_EN	**Enables PWM of ACCDET voltage threshold unit** Disabled in TV mode 1'b0: Disable 1'b1: Enable
0	ACCDET_CMP_PWM_EN	**Enables PWM of ACCDET comparator** 1'b0: Disable 1'b1: Enable

0F1A **ACCDET_CON3** **ACCDET Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_PWM_WIDTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_PWM_WIDTH	**ACCDET PWM width** PWM output frequency = 32,768/(PWM_WIDTH+1)Hz

0F1C **ACCDET_CON4** **ACCDET Control Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_PWM_THRESH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_PWM_THRESH	**ACCDET PWM threshold** PWM output duty cycle = (PWM_THRESH+1)/(PWM_WIDTH+1) PWM output high time = (PWM_THRESH+1)/32,768 sec

0F1E **ACCDET_CON5** **ACCDET Control Register 5** **0101**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_FALL_DELAY	ACCDET_RISE_DELAY														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit(s)	Name	Description

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Bit(s)	Name	Description
15	ACCDET_FALL_DELAY	**Falling delay cycle compared to PWM waveform** To make sure the plug state is stable after ACCDET is disabled, the suitable falling delay cycle is necessary.
14:0	ACCDET_RISE_DELAY	**Rising delay cycle compared to PWM waveform** To make sure the plug state is stable before ACCDET is enabled, the suitable rising delay cycle is necessary.

0F20 ACCDET_CON6 ACCDET Control Register 6 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE0	**De-bounce time control of state 0** De-bounce time = (DEBOUNCE/freq) sec In TV mode, freq is bus clock and 32,768Hz in the MIC mode.

0F22 ACCDET_CON7 ACCDET Control Register 7 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE1	**De-bounce time control of state 1** De-bounce time = (DEBOUNCE/freq) sec In TV mode, freq is bus clock and 32,768Hz in the MIC mode.

0F24 ACCDET_CON8 ACCDET Control Register 8 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE2	**De-bounce time control of state 2** De-bounce time = (DEBOUNCE/freq) sec In TV mode, freq is bus clock 32,768Hz in the MIC mode.

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0F26	ACCDET_CON9	ACCDET Control Register 9	0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE3	**De-bounce time control of state 3** De-bounce time = (DEBOUNCE/freq) sec In TV mode, freq is bus clock 32,768Hz in the MIC mode.

0F28	ACCDET_CON10	ACCDET Control Register 10	0005

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_DEBOUNCE4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit(s)	Name	Description
15:0	ACCDET_DEBOUNCE4	De-bounce time to control AUXADC when in state 0

0F2C	ACCDET_CON12	ACCDET Control Register 12	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_EINT_IRQ_POLARITY					ACCDET_EINT_IRQ_CLR	ACCDET_NEGV_IRQ_CLR	ACCDET_IRQ_CLR						ACCDET_EINT_IRQ	ACCDET_NEGV_IRQ	ACCDET_IRQ
Type	RW					RW	RW	RW						RO	RO	RO
Reset	0					0	0	0						0	0	0

Bit(s)	Name	Description
15	ACCDET_EINT_IRQ_POLARITY	**ACCDET EINT IRQ polarity** 1'b0: Falling edge 1'b1: Rising edge
10	ACCDET_EINT_IRQ_CLR	**Clears ACCDET_EINT interrupt status** When ACCDET_EINT interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status. This bit will pause all activities of ACCDET_EINT design until both the interrupt status and IRQ_CLR are cleared.
9	ACCDET_NEGV_IRQ_CLR	**Clears ACCDET_NEGV interrupt status** When ACCDET_NEGV interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status. This bit will pause all activities of ACCDET_NEGV design until both the interrupt status and IRQ_CLR are cleared.

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Bit(s)	Name	Description
8	ACCDET_IRQ_CLR	**Clears ACCDET interrupt status** When ACCDET interrupt is asserted, IRQ_CLR must be set to 1 to clear the interrupt status. This bit will pause all activities of ACCDET design until both the interrupt status and IRQ_CLR are cleared.
2	ACCDET_EINT_IRQ	**Clears ACCDET_EINT interrupt status**
1	ACCDET_NEGV_IRQ	**Clears ACCDET_NEGV interrupt status**
0	ACCDET_IRQ	**ACCDET interrupt status** Due to this register is cleared by the hardware, the interrupt edge-sensitive scheme should be adopted for this design.

0F30 **ACCDET_CON14** **ACCDET Control Register 14** **00FF**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_AUDACCDETAUXADCSWCTRL	ACCDET_CMP_CLK	ACCDET_VTH_CLK	ACCDET_MBIAS_CLK												
Type	RO	RO	RO	RO												
Reset	0	0	0	0												

Bit(s)	Name	Description
15	DA_AUDACCDETAUXADCSWCTRL	Controls ACCDET to AUXADC switch
14	ACCDET_CMP_CLK	Turns on comparator for accessory detection
13	ACCDET_VTH_CLK	Turns on threshold voltage for accessory detection
12	ACCDET_MBIAS_CLK	Turns on earphone bias voltage for accessory detection

0F32 **ACCDET_CON15** **ACCDET Control Register 15** **0061**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			ACCDET_EINT_PWM_WIDTH			ACCDET_EINT_PWM_THRESH				ACCDET_EINT_DEBOUNCE						
Type			RW			RW				RW						
Reset			0	0		0	0	0		1	1	0				

Bit(s)	Name	Description
13:12	ACCDET_EINT_PWM_WIDTH	**ACCDET EINT PWM width** 2'b00: 4ms 2'b01: 8ms 2'b10: 16ms

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Bit(s)	Name	Description
		2'b11: 32ms
10:8	ACCDET_EINT_PWM_THRESH	**ACCDET EINT PWM threshold** 3'b000: 0.5ms 3'b001: 1ms 3'b010: 2ms 3'b011: 3ms 3'b100: 4ms 3'b101: 8ms 3'b110: 16ms 3'b111: 32ms
6:4	ACCDET_EINT_DEBOUNCE	**ACCDET EINT debounce time** 3'b000: 1ms 3'b001: 2ms 3'b010: 4ms 3'b011: 8ms 3'b100: 16ms 3'b101: 32ms 3'b110: 256ms 3'b111: 512ms

0F34 ACCDET_CON16 ACCDET Control Register 16 0161

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACCDET_EINT_PWM_RISE_DELAY										ACCDET_EINT_PWM_FALL_DELAY	ACCDET_NEGV_THRESH				
Type	RW										RW	RW				
Reset	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	1

Bit(s)	Name	Description
15:6	ACCDET_EINT_PWM_RISE_DELAY	**Rising delay cycle compared to PWM waveform** To make sure the plug state is stable before ACCDET_EINT is enabled, the suitable rising delay cycle is necessary.
5	ACCDET_EINT_PWM_FALL_DELAY	**Falling delay cycle compared to PWM waveform** To make sure the plug state is stable after ACCDET_EINT is disabled, the suitable falling delay cycle is necessary.
4:0	ACCDET_NEGV_THRESH	**ACCDET NVG debounce threshold** 5'd0: 1/32 5'd1: 2/32 5'd2: 3/32 5'd3: 4/32 5'dN: (N+1)/32

0F3A ACCDET_CON19 ACCDET Control Register 19 0000

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NI_EINTCMPEN	EINTCMPOUT	NVDETECTOUT													
Type	RO	RO	RO													
Reset	0	0	0													

Bit(s)	Name	Description
15	NI_EINTCMPEN	
14	EINTCMPOUT	
13	NVDETECTOUT	

0F48 CHR_CON0 Charger Control Register 0 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RGS_VCDT_HV_DET		RGS_CHRDET	RG_CHR_EN	RG_CSDAC_EN		RGS_CHR_LDO_DET	RG_VCDT_HV_EN
Type									RO		RO	RW	RW		RO	RW
Reset									0		0	0	0		0	1

Bit(s)	Name	Description
7	RGS_VCDT_HV_DET	**Detects charger-in high voltage (with de-bounce)** 0: Charge-in voltage < VCDT_HV_VTH 1: Charge-in voltage > VCDT_HV_VTH
5	RGS_CHRDET	**Detects charger-in** 0: No valid charger detected 1: Valid charger detected
4	RG_CHR_EN	**Charger enable setting** Will gate CSDAC_EN, PCHR_AUTO and HWCV_EN. 0: Disable charger 1: Enable charger
3	RG_CSDAC_EN	**Enables CS DAC** 0: Disable CS DAC 1: Enable CS DAC
1	RGS_CHR_LDO_DET	**Detects charger LDO** If not detected, pulse charger cannot work. 0: Invalid charger LDO 1: Valid charger LDO
0	RG_VCDT_HV_EN	**Enables ChargerIn HV detection function** 0: Disable 1: Enable

0F4A CHR_CON1 Charger Control Register 1 00F2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_VCDT_HV_VTH				RG_VCDT_LV_VTH			
Type									RW				RW			
Reset									1	1	1	1	0	0	1	0

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Bit(s)	Name	Description
7:4	RG_VCDT_HV_VTH	**ChargerIn HV detection threshold** Default 4.3/9.5V for VTHL/VTHH. 0000~1000: 4.2V~4.6V with 50mV/step 1001~1100: 6V~7.5V with 500mV/step 1101~1111: 8.5V~10.5V with 1000mV/step
3:0	RG_VCDT_LV_VTH	**ChargerIn LV detection threshold** Default 4.3/9.5V for VTHL/VTHH. 0000~1000: 4.2V~4.6V with 50mV/step 1001~1100: 6V~7.5V with 500mV/step 1101~1111: 8.5V~10.5V with 1000mV/step

0F4C **CHR_CON2** **Charger Control Register 2** **0004**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RGS_VBAT_CC_DET**	**RGS_VBAT_CV_DET**	**RGS_CS_DET**		**RG_CS_EN**	**RG_VBAT_CC_EN**	**RG_VBAT_CV_EN**	
Type									RO	RO	RO		RW	RW	RW	
Reset									0	0	0		0	1	0	

Bit(s)	Name	Description
7	RGS_VBAT_CC_DET	**Detects VBAT voltage for CC** 0: VBAT voltage < VBAT_CC_VTH 1: VBAT voltage > VBAT_CC_VTH
6	RGS_VBAT_CV_DET	**Detects VBAT voltage for CV** 0: VBAT voltage < VBAT_CV_VTH 1: VBAT voltage > VBAT_CV_VTH
5	RGS_CS_DET	**Detects current sense voltage** 0: CS voltage < CS_VTH 1: CS voltage > CS_VTH
3	RG_CS_EN	**Enables current sense voltage detection comparator** 0: Disable 1: Enable
2	RG_VBAT_CC_EN	**Enables battery CC detection**
1	RG_VBAT_CV_EN	**Enables battery CV detection** 0: Disable 1: Enable

0F4E **CHR_CON3** **Charger Control Register 3** **00CD**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RG_VBAT_CC_VTH**			**RG_VBAT_CV_VTH**				
Type									RW			RW				
Reset									1	1		0	1	1	0	1

Bit(s)	Name	Description

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Bit(s)	Name	Description
7:6	RG_VBAT_CC_VTH	**Battery CC detection threshold** 00: 3.3V 01: 3.35V 10: 3.4V 11: 3.45V (default)
4:0	RG_VBAT_CV_VTH	**Battery CV detection threshold trimming option** Default 4.2V. For FT CV threshold trimming but not for fine tuning (pchr_dig should invert MSB bit; otherwise, BC1.1 2.2V threshold will be wrong.) 00000: 3.7750V 00001: 3.8000V 00010: 3.8500V 00011: 3.9000V 00100: 4.0000V 00101: 4.0500V 00110: 4.1000V 00111: 4.1250V 01000: 4.1375V 01001: 4.1500V 01010: 4.1625V 01011: 4.1750V 01100: 4.1875V 01101: 4.2000V (default) 01110: 4.2125V 01111: 4.2250V 10000: 4.2375V 10001: 4.2500V 10010: 4.2625V 10011: 4.2750V 10100: 4.3000V 10101: 4.3250V 10110: 4.3500V 10111: 4.3750V 11000: 4.4400V 11001: 4.4250V 11111: 2.2V (used in BC1.1 application)

0F50 **CHR_CON4** **Charger Control Register 4** **000F**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_CS_VTH			
Type													RW			
Reset													1	1	1	1

Bit(s)	Name	Description
3:0	RG_CS_VTH	**Current sense voltage detection threshold @ Rcs=56mohm** 1111: 70mA 1110: 200mA 1101: 300mA 1100: 450mA (usbdl) 1011: 550mA 1010: 650mA 1001: 700mA 1000: 800mA 0111: 900mA 0110: 1000mA 0101: 1100mA 0100: 1200mA

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Bit(s)	Name	Description
		0011: 1350mA 0010: 1500mA 0001: 1600mA 0000: 2000mA

0F54 CHR_CON6 Charger Control Register 6 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RGS_VBAT_OV_DET	RG_VBAT_OV_DEG		RG_VBAT_OV_VTH			RG_VBAT_OV_EN
Type										RO	RW		RW			RW
Reset										0	0		0	0	0	1

Bit(s)	Name	Description
6	RGS_VBAT_OV_DET	**Detects VBAT_OV voltage** 0: VBAT voltage < VBAT_OV_VTH 1: VBAT voltage > VBAT_OV_VTH
5	RG_VBAT_OV_DEG	**Enables VBAT OV voltage detection deglitch** 0: No debounce 1: Debounce one cycle (1us)
3:1	RG_VBAT_OV_VTH	**Battery over-voltage detection threshold (H/L)** 000: 4.200V/4.150V (default) 001: 4.300V/4.250V 010: 4.400V/4.350V 011: 4.450V/4.400V 1xx: 3.800V/3.800V
0	RG_VBAT_OV_EN	**Battery over-voltage for driving protection** 0: Disable 1: Enable

0F56 CHR_CON7 Charger Control Register 7 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_BATON_TDET_EN						BATON_TDET_EN	RG_BATON_HT_EN_RSV0	RG_BATON_EN
Type								RW						RW	RW	RW
Reset								0						0	0	1

Bit(s)	Name	Description
8	RG_BATON_TDET_EN	**Enables BATON temperature detection via AUXADC** (Gated by CHR_LDO_DET to default 0 in analog domain). This RG is also used to enable external SWCHR BATON detection. 0: Disable temperature detection related TREF power switch 1: Enable temperature detection related TREF power switch (SW should enable AUXADC reference buffer before enabling this switch)

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Bit(s)	Name	Description
2	BATON_TDET_EN	**0: N/A** 1: Enable BATON temperature detection
1	RG_BATON_HT_EN_RSV0	**Detects battery-on HW high temperature** 0: Disable 1: Enable
0	RG_BATON_EN	**Enables BATON battery detection comparator** (Gated by CHR_LDO_DET to default 1 in analog domain) 0: Disable 1: Enable (default)

0F5A CHR_CON9 Charger Control Register 9 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_FRC_CSVTH_USBDL
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_FRC_CSVTH_USBDL	**Forces CS DAC detection threshold to maximum in USB download mode** 0: CS_VTH=450mA in USBDL mode 1: CS_VTH=1600mA in USBDL mode

0F5C CHR_CON10 Charger Control Register 10 0020

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RGS_OTG_BVALID_DET	RG_OTG_BVALID_EN					
Type										RO	RW					
Reset										0	1					

Bit(s)	Name	Description
6	RGS_OTG_BVALID_DET	**Indicates if the session for B-peripheral is valid (0.8V<Vth<4V). Here VBUS is connected to CHRIN** 0: Vbus < 0.8V 1: Vbus > 4V
5	RG_OTG_BVALID_EN	**Enables OTG BValid detection** 0: Disable 1: Enable

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0F60 CHR_CON12 Charger Control Register 12 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_PCHR_FT_CTRL						
Type										RW						
Reset										0	0	0				

Bit(s)	Name	Description
6:4	RG_PCHR_FT_CTRL	**FT control bits** Bit[2]: Extend charger detection duration 10ms Bit[1]: Force TOH/TOL = 3ms/1ms Bit[0]: Always turn on charger detection (VCDT)

0F62 CHR_CON13 Charger Control Register 13 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_CHRWDT_WR				RG_CHRWDT_EN	RG_CHRWDT_TD			
Type								RW				RW	RW			
Reset								0				1	0	0	0	0

Bit(s)	Name	Description
8	RG_CHRWDT_WR	**Resets charger watchdog timer and updates CHRWDT_TD** 0: Reset inactive 1: Reset active and CHRWDT_TD updated to PCHR_DIG
4	RG_CHRWDT_EN	**Enables charger watchdog timer** Note: UVLO doesn't care this bit and will time out after 3000s. PCHR_TESTMODE can be forced to control watchdog enable by using this bit. 0: Disable 1: Enable if (CHR_EN(@CHR_CON0) = 1)
3:0	RG_CHRWDT_TD	**Time constant setting for charger watchdog timer** 0: 4 sec 1: 8 sec 2: 16 sec 3: 32 sec 4: 128 sec 5: 256 sec 6: 512 sec 7: 1024 sec 8~15: 3000 sec

0F64 CHR_CON14 Charger Control Register 14 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_PCHR_RV							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
7:0	RG_PCHR_RV	Reserved for tests

0F66 CHR_CON15 Charger Control Register 15 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RGS_CHRWDT_OUT	RG_CHRWDT_FLAG_WR	RG_CHRWDT_INT_EN
Type														RO	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	RGS_CHRWDT_OUT	**Timeout flag for charger watchdog timer** Read: 0: No timeout status 1: Assert timeout status
1	RG_CHRWDT_FLAG_WR	**Clears timeout flag for charger watchdog timer** Read: 0: N/A (while RGS_CHRWDT_OUT=0) 1: Clear timeout flag when RGS_CHRWDT_OUT=1
0	RG_CHRWDT_INT_EN	**Interrupt enable setting for charger watchdog timer** 0: Disable 1: Enable

0F68 CHR_CON16 Charger Control Register 16 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RG_ADCIN_CHR_EN	RG_ADCIN_VSEN_EN	RG_ADCIN_VBAT_EN	RG_ADCIN_VSEN_EXT_BATON_EN	RG_ADCIN_VSEN_MUX_EN					RG_USBDL_SET	RG_USBDL_RST		
Type				RW	RW	RW	RW	RW					RW	RW		
Reset				0	0	0	0	0					0	0		

Bit(s)	Name	Description
12	RG_ADCIN_CHR_EN	**Enables AUXADC input source for CHR** 0: Disable 1: Enable
11	RG_ADCIN_VSEN_EN	**Enables AUXADC input source for VSEN** 0: Disable 1: Enable
10	RG_ADCIN_VBAT_EN	**Enables AUXADC input source for VBAT** 0: Disable 1: Enable

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Bit(s)	Name	Description
9	RG_ADCIN_VSEN_EXT_BATON_EN	**Enables AUXADC input source for external source to be switched to AUXADC's Ch3** 0: Disable 1: Enable
8	RG_ADCIN_VSEN_MUX_EN	**Enables AUXADC input source for VSEN to be switched to VBAT's divider** 0: Disable 1: Enable
3	RG_USBDL_SET	**Controls USBDL_MODE software setup** 0: No effect 1: Force to enter USBDL mode
2	RG_USBDL_RST	**Controls USBDL_MODE software reset** 0: No effect 1: Force to leave USBDL mode (the priority is lower than USBDL_DET.)

0F6A **CHR_CON17** **Charger Control Register 17** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_UVLO_VH_LAT			RG_UVLO_VTHL				
Type									RW			RW				
Reset									0			0	0	0	1	0

Bit(s)	Name	Description
7	RG_UVLO_VH_LAT	**UVLO VH latch signal** 0: Disable 1: Enable
4:0	RG_UVLO_VTHL	**Selects UVLO low threshold** 00000: 2.5V 00001: 2.55V 00010: 2.6V (default) 00011: 2.65V 00100: 2.7V 00101: 2.75V 00110: 2.8V 00111: 2.85V 01000: 2.9V

0F6C **CHR_CON18** **Charger Control Register 18** **0003**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_LBAT_INT_VTH				
Type												RW				
Reset												0	0	0	1	1

Bit(s)	Name	Description
4:0	RG_LBAT_INT_VTH	**LBAT_INT threshold voltage** 00000: 2.5V

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Bit(s)	Name	Description
		00001: 2.55V 00010: 2.6V (default) 00011: 2.65V 00100: 2.7V 00101: 2.75V 00110: 2.8V 00111: 2.85V 01000: 2.9V 01001: 2.95V 01010: 3.0V 01011: 3.05V 01100: 3.1V 01101: 3.15V 01110: 3.2V 01111: 3.25V 11000: 3.3V 11001: 3.35V 11010: 3.4V

0F6E **CHR_CON19** **Charger Control Register 19** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**RG_BGR_UNCHOP**	**RG_BGR_UNCHOP_PH**		**RG_BGR_RSEL**		
Type											RW	RW		RW		
Reset											0	0		0	0	0

Bit(s)	Name	Description
5	RG_BGR_UNCHOP	**BGR unchop mode** 0: Chop mode 1: Unchop mode
4	RG_BGR_UNCHOP_PH	**Selects BGR unchop mode phase** 0: Select phase 0 path in unchop mode 1: Select phase 1 path in unchop mode
2:0	RG_BGR_RSEL	**Selects BGR resistor (R0 = R1)** R2=85K, and VBG=(R0/R2)*dVBE+VBE 0: c0, 780K (default) 1: c1, 820K 2: c2, 860K 3: c3, 900K 4: cm4, 620K 5: cm3, 660K 6: cm2, 700K 7: cm1, 740K

0F70 **CHR_CON20** **Charger Control Register 20** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RGS_BC11_C**				**RG_BC11_VSRC_EN**		**RG_BC11_RS**	**RG_BC11_BB**

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									MP_ OUT						T	_CT RL
Type									RO				RW		RW	RW
Reset									0				0	0	0	0

Bit(s)	Name	Description
7	RGS_BC11_CMP_OUT	**Detects comparison result of BC11 charger** 0: DP or DM < BC11_VREF_VTH 1: DP or DM > BC11_VREF_VTH
3:2	RG_BC11_VSRC_EN	**BC11 voltage source** Set VDP_SRC = 0.6V. 0: Disable voltage 1: Enable voltage source to DM 2: Enable voltage source to DP 3: Forbidden
1	RG_BC11_RST	**Resets BC11 detection mechanism in PCHR_DIG** 0: No effect 1: BC11 detection mechanism is disabled in PCHR_DIG.
0	RG_BC11_BB_CTRL	**Forces BC11 charger detection controlled by baseband** 0: BC11 detection by PCHR_DIG (hardware mode) 1: BC11 detection by baseband (software mode)

0F72 **CHR_CON21** **Charger Control Register 21** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_BC11_BIAS_EN	RG_BC11_IPU_EN		RG_BC11_IPD_EN		RG_BC11_CMP_EN		RG_BC11_VREF_VTH	
Type								RW	RW		RW		RW		RW	
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	RG_BC11_BIAS_EN	**Enables BC11 detection bias circuit** 0: Disable 1: Enable
7:6	RG_BC11_IPU_EN	**Enables BC11 7~15uA pull up current** 0: Disable pull-up current 1: Enable pull-up current to DM 2: Enable pull-up current to DP 3: Forbidden
5:4	RG_BC11_IPD_EN	**BC11 50~150uA pull-down current** 0: Disable pull-down current 1: Enable pull-down current to DM 2: Enable pull-down current to DP 3: Forbidden
3:2	RG_BC11_CMP_EN	**BC11 comparator connection** 0: Disable comparator 1: Enable comparator to DM 2: Enable comparator to DP 3: Forbidden
1:0	RG_BC11_VREF_VTH	**VREF threshold voltage for comparator** 0: VREF_VTH=0.325V

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Bit(s)	Name	Description
		1: VREF_VTH=1.2V 2, 3: VREF_VTH=2.6V (for Apple adaptor)

0F74 **CHR_CON22** **Charger Control Register 22** **0022**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_CSDAC_STP_DEC				RG_CSDAC_STP_INC		
Type										RW				RW		
Reset										0	1	0		0	1	0

Bit(s)	Name	Description
6:4	RG_CSDAC_STP_DEC	**CV HW Mode decreased code per step** 1/1/2/3/4/5/6/7 code/ per-step
2:0	RG_CSDAC_STP_INC	**CV HW Mode increased code per step** 1/1/2/3/4/5/6/7 code/ per-step

0F76 **CHR_CON23** **Charger Control Register 23** **0024**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_CSDAC_STP				RG_CSDAC_DLY		
Type										RW				RW		
Reset										0	1	0		1	0	0

Bit(s)	Name	Description
6:4	RG_CSDAC_STP	**Current DAC output step timer** 1/1/2/3/4/5/6/7 code/ per-step
2:0	RG_CSDAC_DLY	**Controls current DAC output detection delay** 16/32/64/128/256/512/1024/2048us (512us default, reused in HW CV mode)

0F78 **CHR_CON24** **Charger Control Register 24** **0044**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CHRIND_DIMMING	RG_CHRIND_ON	RG_LOW_ICH_DB					
Type									RW	RW	RW					
Reset									0	1	0	0	0	1	0	0

Bit(s)	Name	Description
7	RG_CHRIND_DIMMING	**Enables pre-charge indicator dimming** 0: Disable 1: Enable
6	RG_CHRIND_ON	**Pre-charge indicator on**

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Bit(s)	Name	Description
		(Gated by CHR_LDO_DET to default 0 in analog domain) 0: Disable indicator 1: Enable indicator
5:0	RG_LOW_ICH_DB	**Plug out HW detection debounce time (base=16ms)** Debounce time: Code*16ms

0F7A CHR_CON25 Charger Control Register 25 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_ULC_DET_EN	RG_HWCV_EN		RG_TRACKING_EN		RG_CSDAC_MODE	RG_VCDT_MODE	RG_CV_MODE
Type									RW	RW		RW		RW	RW	RW
Reset									0	0		1		0	0	0

Bit(s)	Name	Description
7	RG_ULC_DET_EN	**Enables charger plug-out auto detection** This function has to be applied with RG_HWCV_EN=1. 0: Disable 1: Enable
6	RG_HWCV_EN	**Enables hardware CV current tracking** 0: Disable 1: Enable
4	RG_TRACKING_EN	**0: Current calibration use CS_VTH[n] and CS_VTH[n-1] as high/low threshold.** 1: Current calibration use CS_VTH[n] and LTH as high/low threshold.
2	RG_CSDAC_MODE	**0: If not entering CC, charging is in AUTO mode.** 1: If leaving UVLO, charging is controlled by RG_CSDAC_EN (same as CC mode).
1	RG_VCDT_MODE	**Selects charger detection mode** 0: Charger detection can only be active in off state. 1: Charger detection is active in both on and off state.
0	RG_CV_MODE	**Selects battery CV detection mode** 0: CV detection can only be active in off state. 1: CV detection is active in both on and off state.

0F7C CHR_CON26 Charger Control Register 26 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_ICHRG_TRIM							RG_BGR_TRIM_EN
Type									RW							RW
Reset									0	0	0	0				0

Bit(s)	Name	Description
7:4	RG_ICHRG_TRIM	**Charging current trimming**

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Bit(s)	Name	Description
0	RG_BGR_TRIM_EN	**Enables bandgap trimming** 0: Disable BG trimming and bypass voltage buffer 1: Enable BG trimming and voltage buffer

0F7E **CHR_CON27** **Charger Control Register 27** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_BGR_TRIM				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	RG_BGR_TRIM	**Bandgap output voltage trimming** 0~15: VBG=1.205V~1.280V with 5mV/step 16~31: VBG=1.125V~1.200V with 5mV/step

0F80 **CHR_CON28** **Charger Control Register 28** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_OVP_TRIM			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	RG_OVP_TRIM	Battery over-voltage protection threshold trimming

0F82 **CHR_CON29** **Charger Control Register 29** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_BGR_TEST_RSTB	RG_BGR_TEST_EN	QI_BGR_EXT_BUF_EN	RG_CHR_OSC_TRIM				
Type									RW	RW	RW	RW				
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	RG_BGR_TEST_RSTB	**Bandgap reference FT test mode resetb signal** (Also gated by RG_BGR_TEST_EN=0 & PMU_TESTMODE=0) -> GPIO control in test mode 0: Reset 1: Does not reset
6	RG_BGR_TEST_EN	**Bandgap reference FT test mode enable signal** 0: Normal mode 1: Test mode (should combine PMU_TESTMODE=1)
5	QI_BGR_EXT_BUF_EN	**Bandgap reference buffer for external usage (MT8320)** 0: Disable

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Bit(s)	Name	Description
		1: Enable (default)
4:0	RG_CHR_OSC_TRIM	**PCHR 1MHz clock trimming, osc. frequency @ tt25oC w/o trimming** 0: 977.2kHz 1: 938.3kHz 2: 903.0kHz 3: 870.9kHz 4: 841.4kHz 5: 814.5kHz 6: 789.7kHz 7: 766.9kHz 8: 745.9kHz 9: 726.2kHz 10: 708.0kHz 11: 691.1kHz 12: 675.2kHz 13: 660.4kHz 14: 646.6kHz 15: 633.6kHz 16: 3.864MHz 17: 3.222MHz 18: 2.768MHz 19: 2.428MHz 20: 2.164MHz 21: 1.953MHz 22: 1.782MHz 23: 1.639MHz 24: 1.518MHz 25: 1.416MHz 26: 1.327MHz 27: 1.249MHz 28: 1.181MHz 29: 1.121MHz 30: 1.068MHz 31: 1.020MHz

0F84 CHR_CON30 Charger Control Register 30 0055

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_DAC_USBDL_MAX									
Type							RW									
Reset							0	0	0	1	0	1	0	1	0	1

Bit(s)	Name	Description
9:0	RG_DAC_USBDL_MAX	**USBDL maximum current setting** Default: 85 => 0001010101

0F86 CHR_CON31 Charger Control Register 31 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PCHR_CM_VDEC_ST				RG_CM_VDEC_TRIG

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												ATUS				
Type												RO				RW
Reset												0				0

Bit(s)	Name	Description
4	PCHR_CM_VDEC_STATUS	**Automatic current procedure status in adaptor output voltage decrement communication mode** 0: Idle 1: Previous trigger is done
0	RG_CM_VDEC_TRIG	**Automatic current procedure trigger in adaptor output voltage decrement communication mode** 0: No effect 1: Trigger automatic current procedure in adaptor output voltage decrement communication mode

0F88 CHR_CON32 Charger Control Register 32 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PCHR_CM_VINC_STATUS				RG_CM_VINC_TRIG
Type												RO				RW
Reset												0				0

Bit(s)	Name	Description
4	PCHR_CM_VINC_STATUS	**Automatic current procedure status in adaptor output voltage decrement communication mode** 0: Idle 1: Previous trigger is done
0	RG_CM_VINC_TRIG	**Automatic current procedure trigger in adaptor output voltage increment communication mode** 0: No effect 1: Trigger automatic current procedure in adaptor output voltage increment communication mode

0F8A CHR_CON33 Charger Control Register 33 1D1D

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_CM_VDEC_HPRD2								RG_CM_VDEC_HPRD1					
Type			RW								RW					
Reset			0	1	1	1	0	1			0	1	1	1	0	1

Bit(s)	Name	Description
13:8	RG_CM_VDEC_HPRD2	**2nd high pulse width of the adaptor output voltage decrement communication mode** High pulse width = (Setting+1)*10ms
5:0	RG_CM_VDEC_HPRD1	**1st high pulse width of the adaptor output voltage decrement communication mode**

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Bit(s)	Name	Description
		High pulse width = (Setting+1)*10ms

0F8C CHR_CON34 Charger Control Register 34 091D

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_CM_VDEC_HPRD4								RG_CM_VDEC_HPRD3					
Type			RW								RW					
Reset			0	0	1	0	0	1			0	1	1	1	0	1

Bit(s)	Name	Description
13:8	RG_CM_VDEC_HPRD4	**4th high pulse width of the adaptor output voltage decrement communication mode** High pulse width = (Setting+1)*10ms
5:0	RG_CM_VDEC_HPRD3	**3rd high pulse width of the adaptor output voltage decrement communication mode** High pulse width = (Setting+1)*10ms

0F8E CHR_CON35 Charger Control Register 35 3109

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_CM_VDEC_HPRD6								RG_CM_VDEC_HPRD5					
Type			RW								RW					
Reset			1	1	0	0	0	1			0	0	1	0	0	1

Bit(s)	Name	Description
13:8	RG_CM_VDEC_HPRD6	**6th high pulse width of the adaptor output voltage decrement communication mode** High pulse width = (Setting+1)*10ms
5:0	RG_CM_VDEC_HPRD5	**5th high pulse width of the adaptor output voltage decrement communication mode** High pulse width = (Setting+1)*10ms

0F90 CHR_CON36 Charger Control Register 36 0909

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_CM_VINC_HPRD2								RG_CM_VINC_HPRD1					
Type			RW								RW					
Reset			0	0	1	0	0	1			0	0	1	0	0	1

Bit(s)	Name	Description
13:8	RG_CM_VINC_HPRD2	**2nd high pulse width of the adaptor output voltage increment communication mode** High pulse width = (Setting+1)*10ms
5:0	RG_CM_VINC_HPRD1	**1st high pulse width of the adaptor output voltage increment communication mode** High pulse width = (Setting+1)*10ms

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0F92 CHR_CON37 Charger Control Register 37 1D1D

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_CM_VINC_HPRD4								RG_CM_VINC_HPRD3					
Type			RW								RW					
Reset			0	1	1	1	0	1			0	1	1	1	0	1

Bit(s)	Name	Description
13:8	RG_CM_VINC_HPRD4	**4th high pulse width of the adaptor output voltage increment communication mode** High pulse width = (Setting+1)*10ms
5:0	RG_CM_VINC_HPRD3	**3rd high pulse width of the adaptor output voltage increment communication mode** High pulse width = (Setting+1)*10ms

0F94 CHR_CON38 Charger Control Register 38 311D

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_CM_VINC_HPRD6								RG_CM_VINC_HPRD5					
Type			RW								RW					
Reset			1	1	0	0	0	1			0	1	1	1	0	1

Bit(s)	Name	Description
13:8	RG_CM_VINC_HPRD6	**6th high pulse width of the adaptor output voltage increment communication mode** High pulse width = (Setting+1)*10ms
5:0	RG_CM_VINC_HPRD5	**5th high pulse width of the adaptor output voltage increment communication mode** High pulse width = (Setting+1)*10ms

0F96 CHR_CON39 Charger Control Register 39 0009

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_CM_LPRD					
Type											RW					
Reset											0	0	1	0	0	1

Bit(s)	Name	Description
5:0	RG_CM_LPRD	**Low pulse width in communication mode** Low pulse width = (Setting+1)*10ms

0F98 CHR_CON40 Charger Control Register 40 00AF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_CM_CS_VTHH				RG_CM_CS_VTHL			
Type									RW				RW			
Reset									1	0	1	0	1	1	1	1

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Bit(s)	Name	Description
7:4	RG_CM_CS_VTHH	**Current sense detection high threshold in communication mode** 0000: 2000mA 0001: 1600mA 0010: 1500mA 0011: 1350mA 0100: 1200mA 0101: 1100mA 0110: 1000mA 0111: 900mA 1000: 800mA 1001: 700mA 1010: 650mA 1011: 550mA 1100: 450mA 1101: 300mA 1110: 200mA 1111: 70mA
3:0	RG_CM_CS_VTHL	**Current sense detection low threshold in communication mode** 0000: 2000mA 0001: 1600mA 0010: 1500mA 0011: 1350mA 0100: 1200mA 0101: 1100mA 0110: 1000mA 0111: 900mA 1000: 800mA 1001: 700mA 1010: 650mA 1011: 550mA 1100: 450mA 1101: 300mA 1110: 200mA 1111: 70mA

0F9A **CHR_CON41** **Charger Control Register 41** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_PCHR_RSV							RGS_BATON_UNDET
Type									RW							RO
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:1	RG_PCHR_RSV	**Reserved**
0	RGS_BATON_UNDET	**Battery-On undetected** 0: Detected 1: Not detected

0F9C **CHR_CON42** **Charger Control Register 42** **0000**

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_ENVTEM_EN	RG_ENVTEM_D
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	RG_ENVTEM_EN	**Blocks CHR_DET signal to start_up** 0: N/A 1: Enable write
0	RG_ENVTEM_D	**Blocks CHR_DET signal to start_up** 0: Does not block 1: Block

0F9E BATON_CON0 BATON Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_BATON_HT_EN_DLY_TIME				RG_BATON_HT_EN
Type												RW				RW
Reset												0				0

Bit(s)	Name	Description
4	RG_BATON_HT_EN_DLY_TIME	**BATON high-temperature detection delay time** 1'b0: 6T 1'b1: 12T
0	RG_BATON_HT_EN	**Detects battery-on HW high temperature** 1'b0: disable 1'b1: enable

0FA0 CHR_CON43 Charger Control Register 43 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_CM_VINC_INT_EN		RG_CM_VDEC_INT_EN									
Type					RW		RW									
Reset					0		0									

Bit(s)	Name	Description
11	RG_CM_VINC_INT_EN	Enables pump express VDEC INT

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Bit(s)	Name	Description
9	RG_CM_VDEC_INT_EN	Enables pump express VDEC INT

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4 Application Notes

4.1 Hardware External Shutdown

The following schematic illustrates the hardware external shut-down function for MT6328 to power down when the main chip software crashes.

- Short press PWRKEY or HOMEKEY
  - INT-> EINT -> software control
  - Power-down, sleep mode or the other functions
- Long press shut-down
  - Force power-off of PMU
  - 5/8/11/14 s with < 1% accuracy
  - External reset function with source from:
    - PWRKEY and HOMEKEY both pressed for a long period of time
      - PWRKEY and HOMEKEY do not use same key
    - PWERKEY pressed for a long period of time
    - HOMEKEY pressed for a long period of time
      - Software disables watchdog counter.

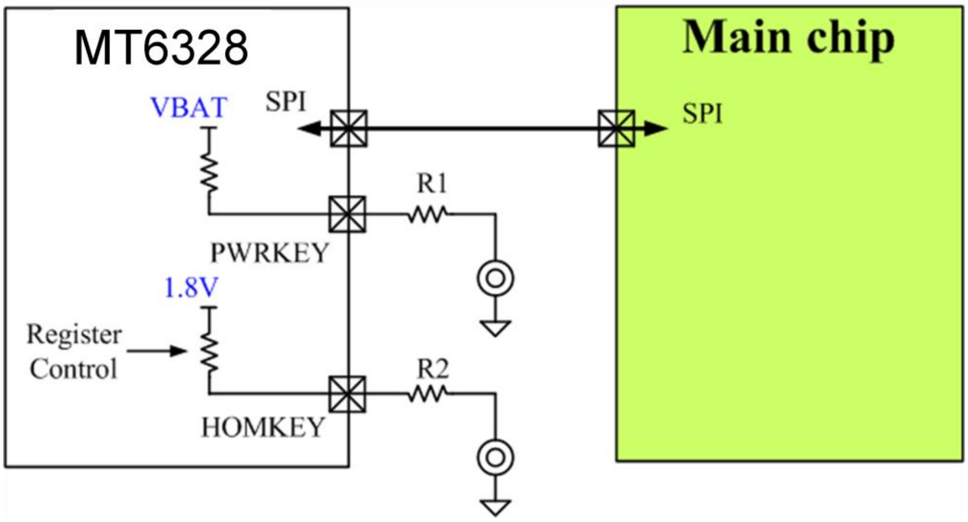

Figure 4-1. Hardware external shut-down function

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4.2 Configuration for Unused Buck Converter

The figure below shows the configuration for MT6328 VPA buck converters that is not used.

- Configuration for VPA not in use:
  - VBAT_PA connect to VBAT; GND_PA connect to GND
  - VPA & VPA_FB: floating
  - RG_VPA_EN = 0 & RG_VPA_NDIS_EN = 1 (software setting)

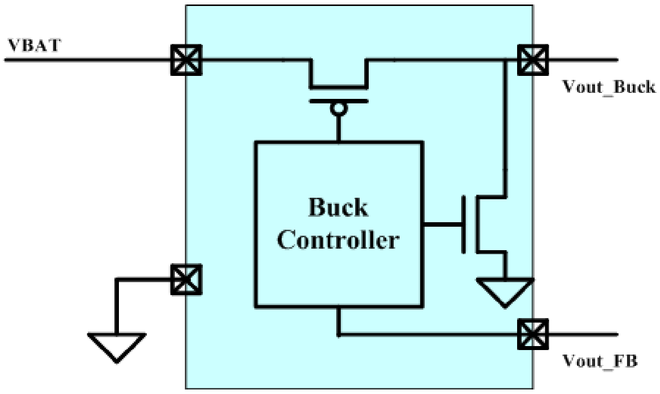

Figure 4-2. Configuration for unused DC/DC

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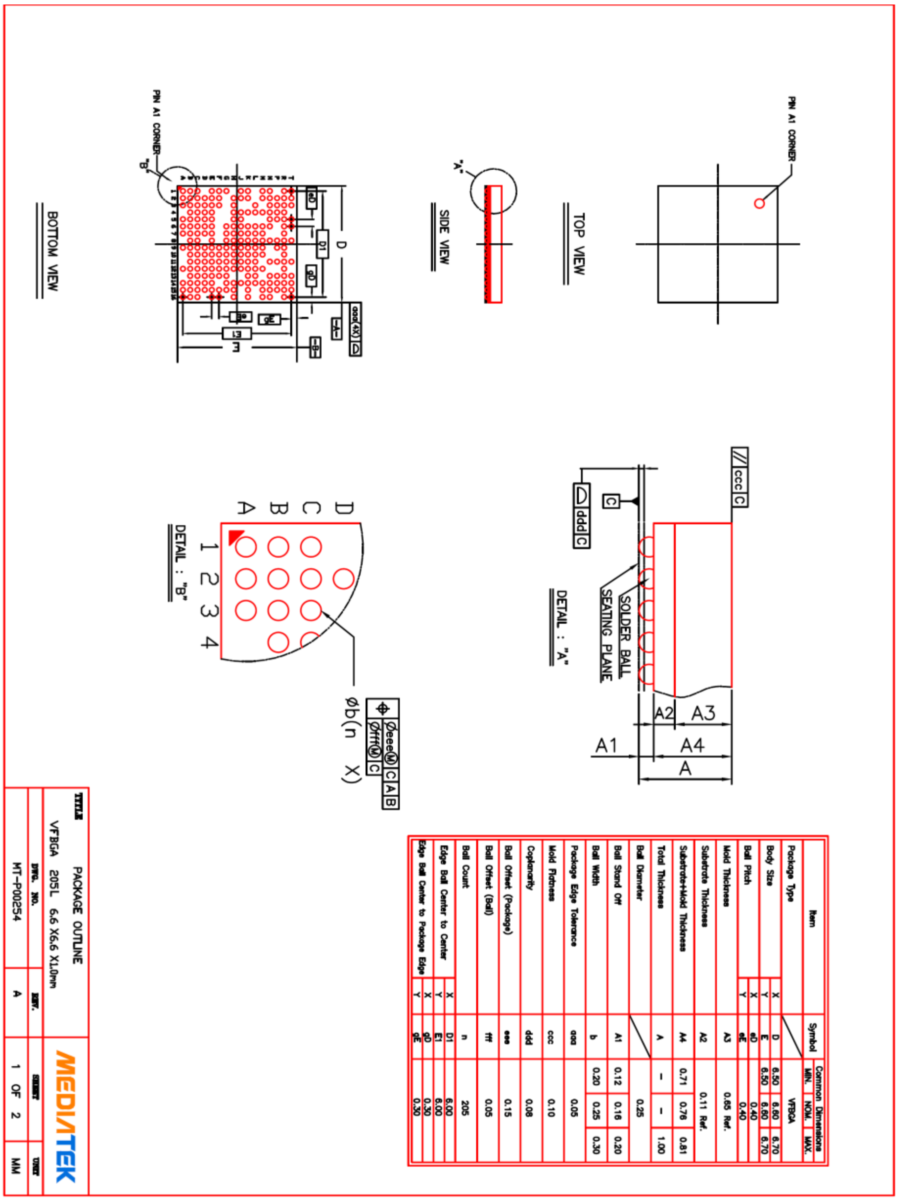
5 MT6328 Packaging

5.1 Package Dimensions



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			VFBGA		
Body Size	X	D	6.50	6.60	6.70
	Y	E	6.50	6.60	6.70
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.65 Ref.	
Substrate Thickness		A2		0.11 Ref.	
Substrate+Mold Thickness		A4	0.71	0.76	0.81
Total Thickness		A	–	–	1.00
Ball Diameter				0.25	
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		205	
Edge Ball Center to Center	X	D1		6.00	
	Y	E1		6.00	
Edge Ball Center to Package Edge	X	gD		0.30	
	Y	gE		0.30	

Figure 5-1. Package dimension

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Appendix

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